360nA I_Q Step Down Converter for Low Power Applications

Check for Samples: TPS62740

FEATURES

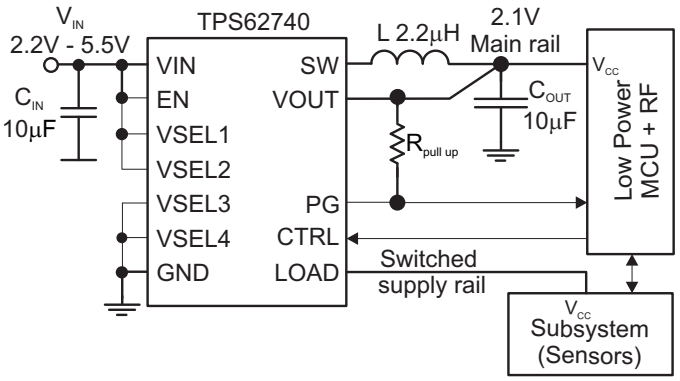
- **Input Voltage Range V_{IN} from 2.2V to 5.5V**
- **Typ. 360nA Quiescent Current**
- **Up to 90% Efficiency at 10µA Output Current**
- **Up to 300mA Output Current**
- **RF Friendly DCS-Control ™**
- **Up to 2 MHz Switching Frequency**
- **Low Output Ripple Voltage**
- **16 Selectable Output Voltages in 100mV Steps between 1.8V to 3.3V**
- **Automatic Transition to No Ripple 100% Mode**
- **Slew Rate Controlled Load Switch**
- **Discharge Function on VOUT / LOAD**
- **Power Good Output**
- **Optimized for Operation with a Tiny 2.2µH Inductor and 10µF C_{OUT}**
- **Total Solution Size <31mm²**
- **Small 2 x 3 mm² SON Package**

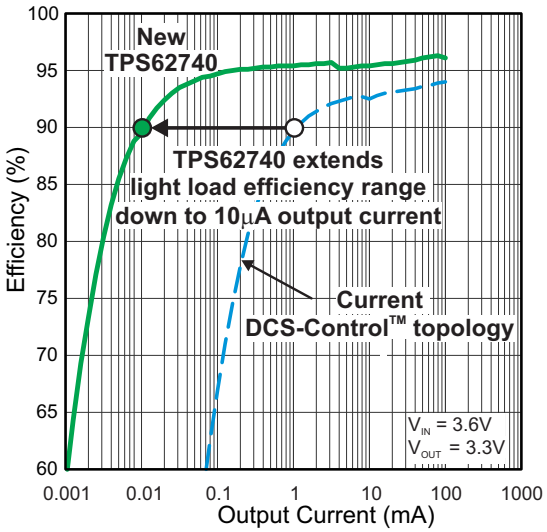
APPLICATIONS

- ***Bluetooth*® Low Energy, RF4CE, Zigbee**
- **Industrial Metering**
- **Energy Harvesting**

DESCRIPTION

The TPS62740 is industry's first step down converter featuring typ. 360nA quiescent current and operating with a tiny 2.2µH inductor and 10µF output capacitor. This new DCS-Control™ based device extends the light load efficiency range below 10µA load currents. It supports output currents up to 300mA. The device operates from rechargeable Li-Ion batteries, Li-primary battery chemistries such as Li-SOCl2, Li-MnO2 and two or three cell alkaline batteries. The input voltage range up to 5.5V allows also operation from a USB port and thin-film solar modules. The output voltage is user selectable by four VSEL pins within a range from 1.8V to 3.3V in 100mV steps. TPS62740 features low output ripple voltage and low noise with a small output capacitor. Once the battery voltage comes close to the output voltage (close to 100% duty cycle) the device enters no ripple 100% mode operation to prevent an increase of output ripple voltage. The device then stops switching and the output is connected to the input voltage. The integrated slew rate controlled load switch provides typ. 0.6Ω on-resistance and can distribute the selected output voltage to a temporarily used sub-system. The TPS62740 is available in a small 12 pin 2 × 3mm² SON package and supports a total solutions size of 31mm².





Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

DCS-Control is a trademark of Texas Instruments.
Bluetooth is a registered trademark of Bluetooth SIG, Inc..

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

T_A	PART NUMBER	Output Voltage setting VSEL 1 - 4	ORDERING(1)	PACKAGE MARKING
–40°C to 85°C	TPS62740	1.8V to 3.3V in 100mV steps	TPS62740DSS	62740
	TPS62741(2)	1.3V to 2.8V in 100mV steps	-/-	-/-

(1) The DSS package is available in tape on reel. Add R suffix to order quantities of 3000 parts per reel, T suffix for 250 parts per reel.
(2) Device option, contact TI for more details

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range (unless otherwise noted)

			VALUE		UNIT
			MIN	MAX	
Pin voltage range (2)	VIN		- 0.3	6	V
	SW (3)		- 0.3	V_{IN} +0.3V	V
	EN, CTRL, VSEL1-4		- 0.3	V_{IN} +0.3V	V
	PG		- 0.3	V_{IN} +0.3V	V
	VOUT, LOAD		- 0.3	3.7	V
PG pin	I_{PG}	sink current		10	mA
ESD rating(4)	HBM Human body model			2	kV
	CDM Charge device model			1	
Maximum operating junction temperature, T_J			- 40	150	°C
Storage temperature range, T_{stg}			- 65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal GND.
(3) The MAX value V_{IN} +0.3V applies for applicative operation (device switching), DC voltage applied to this pin may not exceed 4V
(4) The human body model is a 100-pF capacitor discharged through a 1.5-kΩ resistor into each pin.

THERMAL INFORMATION

THERMAL METRIC(1)		DSS / 12 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	61.8	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	70.9	
θ_{JB}	Junction-to-board thermal resistance	25.7	
ψ_{JT}	Junction-to-top characterization parameter	1.9	
ψ_{JB}	Junction-to-board characterization parameter	25.7	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	7.2	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

RECOMMENDED OPERATING CONDITIONS

			MIN	NOM	MAX	UNIT
V_{IN}	Supply voltage V_{IN}		2.2		5.5	V
I_{OUT} + I_{LOAD}	Device output current (sum of I_{OUT} and I_{LOAD})	V_{OUTnom} + 0.7V ≤ V_{IN} ≤ 5.5V			300	mA
		V_{OUTnom} ≤ V_{IN} ≤ V_{OUTnom} +0.7V			100	
I_{LOAD}	Load current (current from LOAD pin)				100	
L	Inductance		1.5	2.2	3.3	µH
C_{OUT}	Output capacitance connected to VOUT pin (not including LOAD pin)				22	µF
C_{LOAD}	Capacitance connected to LOAD pin				10	
T_J	Operating junction temperature range		-40		125	°C
T_A	Ambient temperature range		-40		85	

ELECTRICAL CHARACTERISTICS

V_{IN} = 3.6V, T_A = –40°C to 85°C typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SUPPLY							
V_{IN}	Input voltage range			2.2		5.5	V
I_Q	Operating quiescent current	EN = V_{IN}, CTRL = GND, I_{OUT} = 0µA, V_{OUT} = 1.8V, device not switching,			360	1800	nA
		EN = V_{IN}, I_{OUT} = 0mA, CTRL = GND, V_{OUT} = 1.8V , device switching			460		
		EN = V_{IN}, I_{OUT} = 0mA., CTRL = V_{IN}, V_{OUT} = 1.8V, device not switching			12.5		µA
I_{SD}	Shutdown current	EN = GND, shutdown current into V_{IN}			70	1000	nA
		EN = GND, shutdown current into V_{IN}, T_A = 60°C			150	450	
V_{TH_UVLO+}	Undervoltage lockout threshold	Rising V_{IN}			2.075	2.15	V
V_{TH_UVLO-}		Falling V_{IN}			1.925	2	
INPUTS EN, CTRL, VSEL 1-4							
$V_{IH\ TH}$	High level input threshold	2.2V ≤ V_{IN} ≤ 5.5V				1.1	V
$V_{IL\ TH}$	Low level input threshold	2.2V ≤ V_{IN} ≤ 5.5V		0.4			V
I_{IN}	Input bias Current	T_A = 25°C				10	nA
		T_A = –40°C to 85°C				25	
POWER SWITCHES							
$R_{DS(ON)}$	High side MOSFET on-resistance	V_{IN} = 3.6V, I_{OUT} = 50mA			0.6	0.85	Ω
	Low Side MOSFET on-resistance				0.36	0.5	
I_{LIMF}	High side MOSFET switch current limit	2.2V ≤ V_{IN} ≤ 5.5V		480	600	720	mA
	Low side MOSFET switch current limit				600		mA
OUTPUT DISCHARGE SWITCH (VOUT)							
R_{DSCH_VOUT}	MOSFET on-resistance	V_{IN} = 3.6V, EN = GND, I_{OUT} = -10mA into VOUT pin			30	65	Ω
I_{IN_VOUT}	Bias current into VOUT pin	V_{IN} = 3.6V, EN = V_{IN}, VOUT = 2V, CTRL = GND	T_A = 25°C		40	100	nA
			T_A = –40°C to 85°C			1010	
LOAD OUTPUT (LOAD)							
R_{LOAD}	High side MOSFET on-resistance	I_{LOAD} = 50mA, CTRL = V_{IN}, VOUT = 2.0V, 2.2 V ≤ V_{IN} ≤ 5.5V			0.6	1.25	Ω
R_{DSCH_LOAD}	Low side MOSFET on-resistance	CTRL = GND, 2.2V ≤ V_{IN} ≤ 5.5V, I_{LOAD} = - 10mA			30	65	
t_{Rise_LOAD}	V_{LOAD} rise time	Starting with CTRL low to high transition, time to ramp V_{LOAD} from 0V to 95% VOUT = 1.8V, 2.2V ≤ V_{IN} ≤ 5.5V, I_{LOAD} = 1mA			315	800	µs

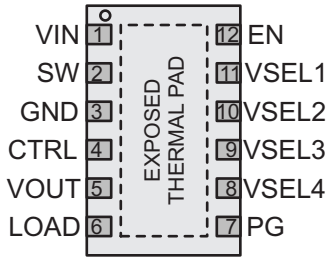
ELECTRICAL CHARACTERISTICS (continued)

V_{IN} = 3.6V, T_A = –40°C to 85°C typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
AUTO 100% MODE TRANSITION							
V_{TH_100+}	Auto 100% Mode leave detection threshold (1)	Rising V_{IN},100% Mode is left with $V_{IN} = V_{OUT} + V_{TH\_100+}$, max value at T_J = 85°C		170	250	340	mV
V_{TH_100-}	Auto 100% Mode enter detection threshold (1)	Falling V_{IN}, 100% Mode is entered with $V_{IN} = V_{OUT} + V_{TH\_100-}$, max value at T_J = 85°C		110	200	280	
POWER GOOD OUTPUT (PG, OPEN DRAIN)							
V_{TH_PG+}	Power good threshold voltage	Rising output voltage on VOUT pin, referred to V_{VOUT}			97.5		%
V_{PG_Hys}		Hysteresis			-3		
V_{OL}	Low level output voltage	2.2V ≤ V_{IN} ≤ 5.5V, EN = GND, current into PG pin I_{PG} = 4mA				0.3	V
I_{IN_PG}	Bias current into PG pin	PG pin is high impedance, VOUT = 2V, EN = V_{IN}, CTRL = GND, I_{OUT} = 0mA	T_A = 25°C		0	10	nA
			T_A = –40°C to 85°C			25	
OUTPUT							
t_{ONmin}	Minimum ON time	V_{IN} = 3.6V, V_{OUT} = 2.0V, I_{OUT} = 0 mA			225		ns
t_{OFFmin}	Minimum OFF time	V_{IN} = 2.3V			50		ns
$t_{Startup\_delay}$	Regulator start up delay time	V_{IN} = 3.6V, from transition EN = low to high until device starts switching			10	25	ms
$t_{Softstart}$	Softstart time with reduced switch current limit	2.2V ≤ V_{IN} ≤ 5.5V, EN = V_{IN}			400	1200	µs
$I_{LIM\_softstart}$	High side MOSFET switch current limit	Reduced switch current limit during softstart		80	150	200	mA
	Low side MOSFET switch current limit				150		
V_{VOUT}	Output voltage range	Output voltages are selected with pins VSEL 1 - 4		1.8		3.3	V
	Output voltage accuracy	V_{IN} = 3.6V, I_{OUT} = 10mA, V_{OUT} = 1.8V		-2.5	0	2.5	%
		V_{IN} = 3.6V, I_{OUT} = 100mA, V_{OUT} = 1.8V		–2	0	2	
	DC output voltage load regulation	V_{OUT} = 1.8V, V_{IN} = 3.6V, CTRL = V_{IN}			0.001		%/mA
	DC output voltage line regulation	V_{OUT} = 1.8V, CTRL = V_{IN}, I_{OUT} = 10 mA, 2.5V ≤ V_{IN} ≤ 5.5V			0		%/V

(1) V_{IN} is compared to the programmed output voltage (V_{OUT}). When V_{IN}–V_{OUT} falls below V_{TH_100-} the device enters 100% Mode by turning the high side MOSFET on. The 100% Mode is exited when V_{IN}–V_{OUT} exceeds V_{TH_100+} and the device starts switching. The hysteresis for the 100% Mode detection threshold V_{TH_100+} - V_{TH_100-} will always be positive and will be approximately 50 mV(typ.)

DSS PACKAGE
(TOP VIEW)



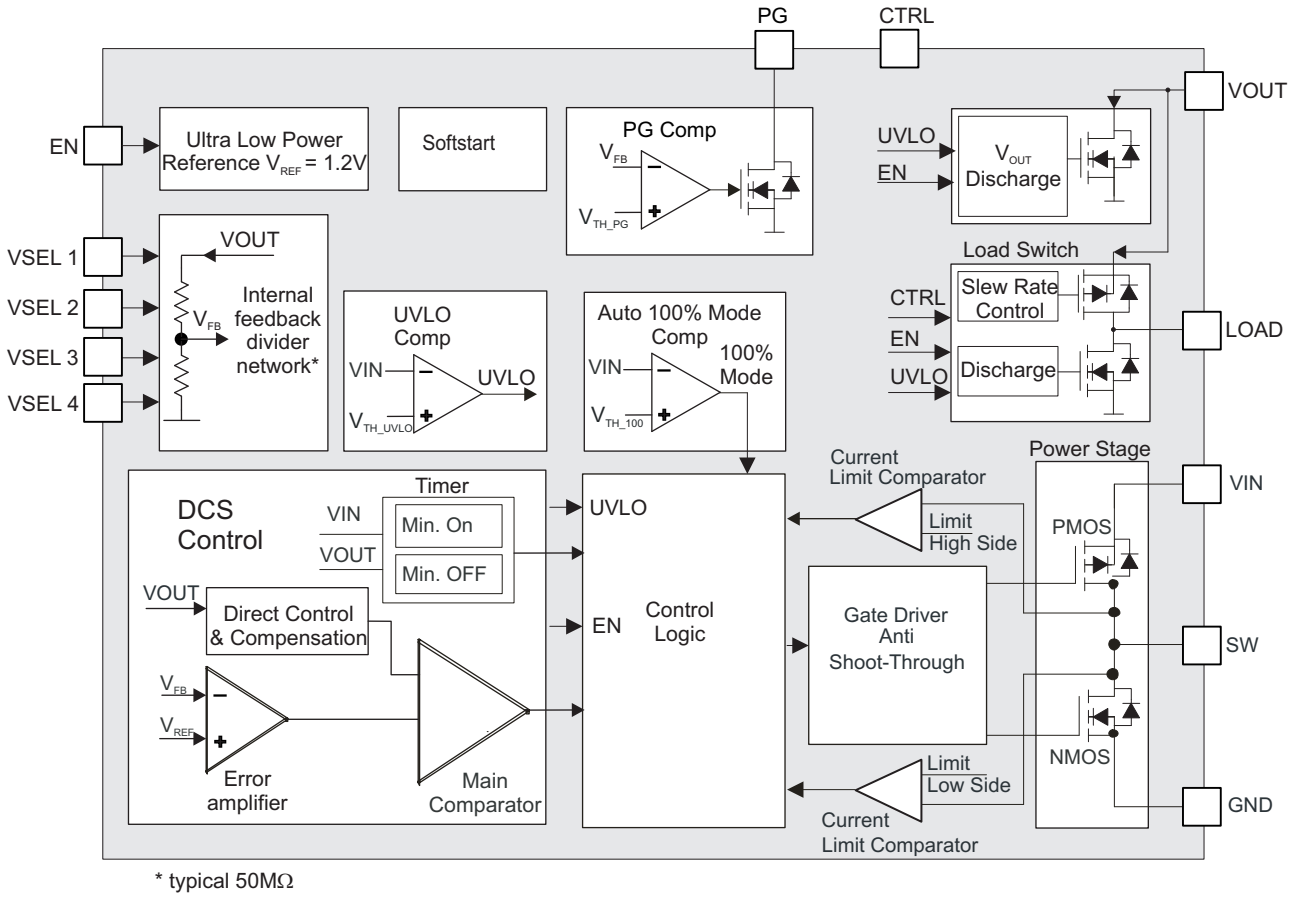
PIN FUNCTIONS

PIN		I/O	DESCRIPTION
NAME	NO		
VIN	1	PWR	V_{IN} power supply pin. Connect this pin close to the VIN terminal of the input capacitor. A ceramic capacitor of 4.7µF is required.
SW	2	OUT	This is the switch pin and is connected to the internal MOSFET switches. Connect the inductor to this terminal.
GND	3	PWR	GND supply pin. Connect this pin close to the GND terminal of the input and output capacitor.
CTRL	4	IN	This pin controls the output LOAD pin. With CTRL = low, the output LOAD is disabled. This pin must be terminated.
VOUT	5	IN	Feedback pin for the internal feedback divider network and regulation loop. An internal load switch is connected between this pin and the LOAD pin. Connect this pin directly to the output capacitor with a short trace.
LOAD	6	OUT	This output is controlled by the CTRL Pin. With CTRL high, an internal load switch connects the LOAD pin to the VOUT pin. The LOAD pin allows to connect / disconnect other system components to the output of the DC/DC converter. This pin is pulled to GND with CTRL pin = low. The LOAD pin features a soft switching. If not used, leave the pin open.
PG	7	OUT	Power good open drain output. This pin is high impedance to indicate "Power Good". Connect a external pull up resistor to generate a "high" level. If not used, this pin can be left open.
VSEL4	8	IN	Output voltage selection pins. See Table 1 for V_{OUT} selection. These pins must be terminated and can be changed during operation.
VSEL3	9	IN	
VSEL2	10	IN	
VSEL1	11	IN	
EN	12	IN	High level enables the devices, low level turns the device into shutdown mode. This pin must be terminated.
EXPOSED THERMAL PAD		NC	Not electrically connected to the IC, but must be soldered. Connect this pad to GND and use it as a central GND plane.

Table 1. OUTPUT VOLTAGE SETTING TPS62740

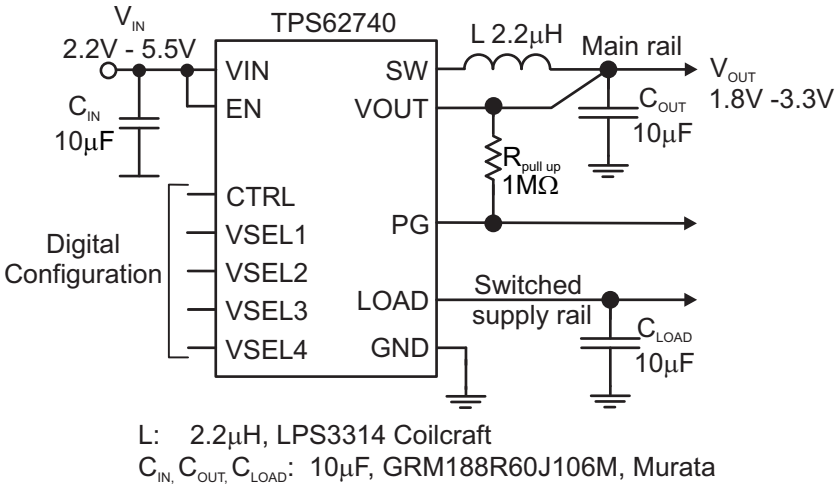
Device	VOUT	VSEL 4	VSEL 3	VSEL 2	VSEL 1
TPS62740	1.8	0	0	0	0
	1.9	0	0	0	1
	2.0	0	0	1	0
	2.1	0	0	1	1
	2.2	0	1	0	0
	2.3	0	1	0	1
	2.4	0	1	1	0
	2.5	0	1	1	1
	2.6	1	0	0	0
	2.7	1	0	0	1
	2.8	1	0	1	0
	2.9	1	0	1	1
	3.0	1	1	0	0
	3.1	1	1	0	1
	3.2	1	1	1	0
	3.3	1	1	1	1

FUNCTIONAL BLOCK DIAGRAM



* typical 50MΩ

PARAMETER MEASUREMENT INFORMATION



L: 2.2µH, LPS3314 Coilcraft
$C_{IN,}$ $C_{OUT,}$ C_{LOAD}: 10µF, GRM188R60J106M, Murata

Figure 1. Measurement configuration with passive components

TYPICAL CHARACTERISTICS

TABLE OF GRAPHS			FIGURE
η	Efficiency	vs Output current	Figure 7, Figure 8, Figure 9, Figure 10
η	Efficiency	vs Input voltage	Figure 11, Figure 12, Figure 13, Figure 14
V_{OUT}	Output voltage	vs Output current	Figure 15, Figure 16, Figure 17, Figure 18
I_{SD}	Shutdown current	vs Input voltage	Figure 3
I_Q	Operating quiescent current	vs Input voltage	Figure 2
$r_{DS(ON)}$	High side MOSFET static drain-source on-state resistance	vs Input voltage and junction temperature	Figure 4
	Low Side MOSFET static drain-source on-state resistance	vs Input voltage and junction temperature	Figure 5
	Load switch on-state resistance	vs Output voltage and junction temperature	Figure 6
	Automatic transition 100% Mode		Figure 25, Figure 26, Figure 27, Figure 48
F_{SW}	Switching frequency	vs Output current	Figure 19, Figure 21, Figure 23
V_{OUT}	Output ripple voltage	vs Output current	Figure 20, Figure 22, Figure 24
	DC/DC steady state typical operation		Figure 28, Figure 29, Figure 30, Figure 31
	Line and load transient performance		Figure 32, Figure 33, Figure 34, Figure 35, Figure 36, Figure 37,
	AC load regulation performance		Figure 38
	LOAD output behavior		Figure 40, Figure 39
	Startup behavior		Figure 41, Figure 42, Figure 43
	Dynamic output voltage scaling		Figure 44
	Input voltage ramp up / down		Figure 45, Figure 46, Figure 47

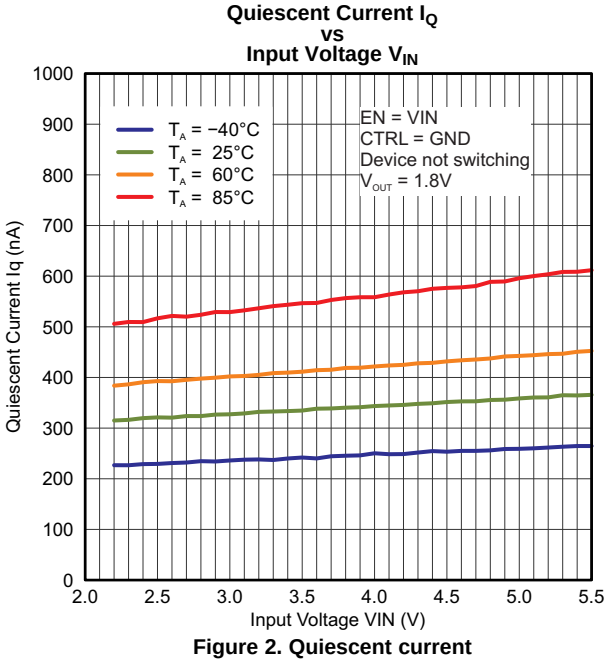


Figure 2. Quiescent current

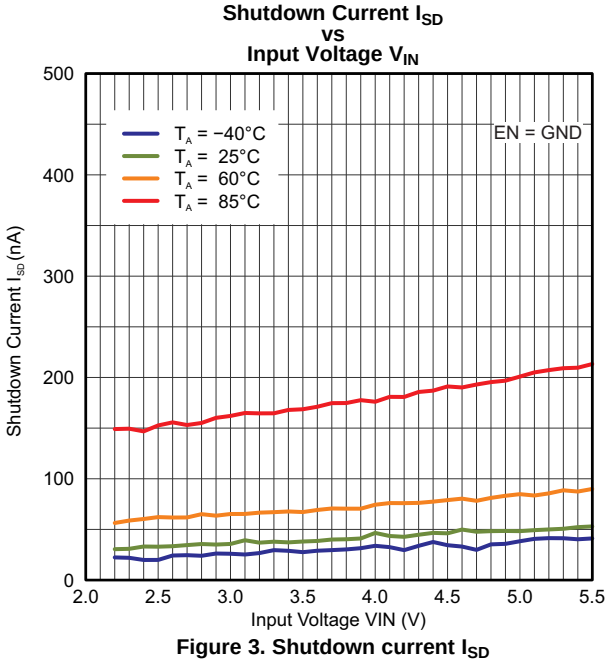


Figure 3. Shutdown current I_{SD}

TYPICAL CHARACTERISTICS (continued)

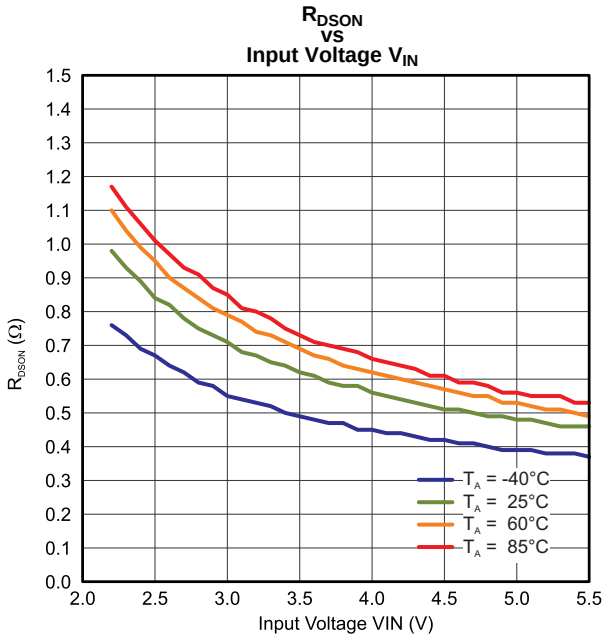


Figure 4. R_{DSON} high side MOSFET

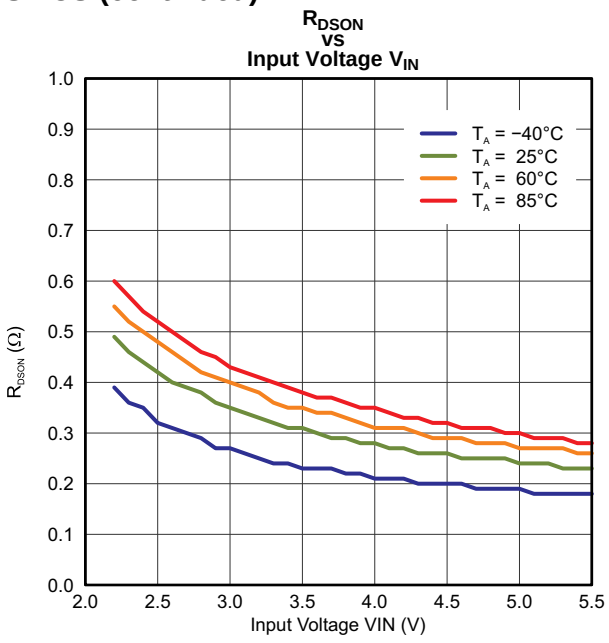


Figure 5. R_{DSON} low side MOSFET

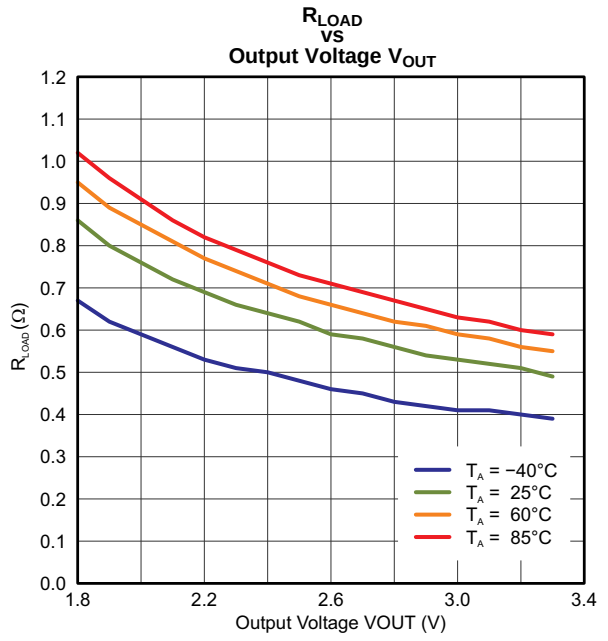


Figure 6. LOAD switch resistance R_{LOAD}

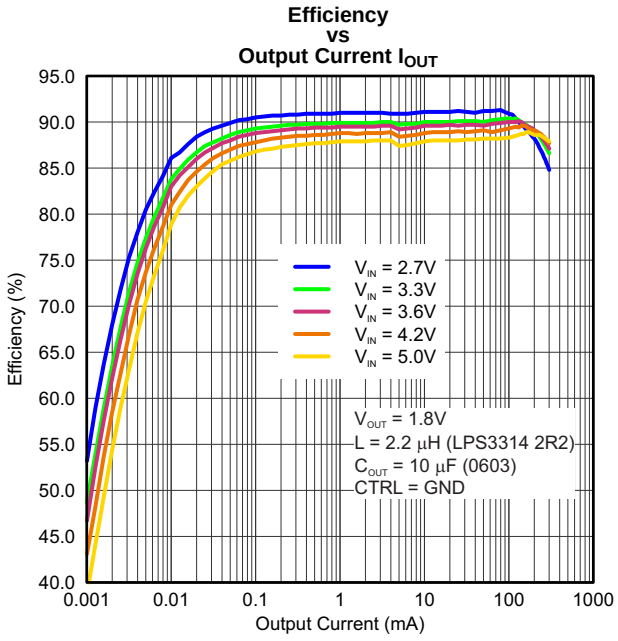


Figure 7. Efficiency V_{OUT} = 1.8V

TYPICAL CHARACTERISTICS (continued)

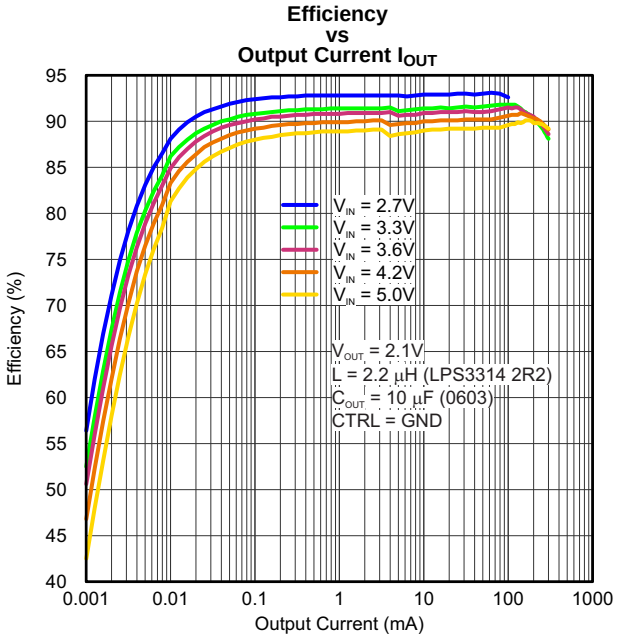


Figure 8. Efficiency V_{OUT} = 2.1V

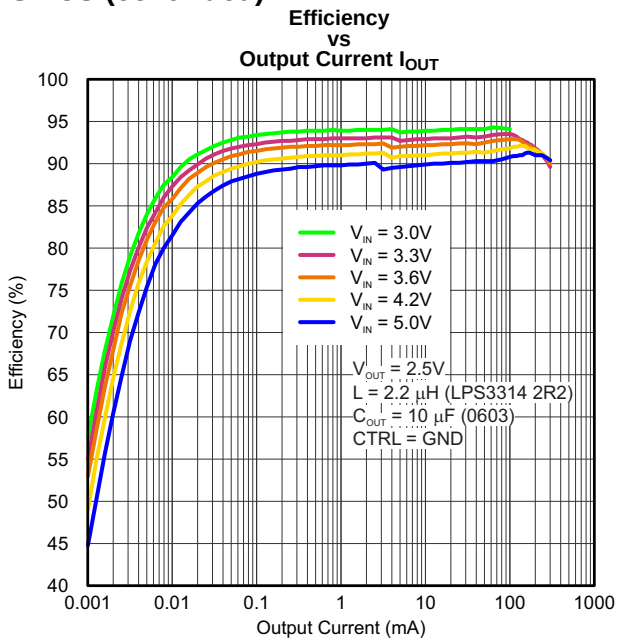


Figure 9. Efficiency V_{OUT} = 2.5V

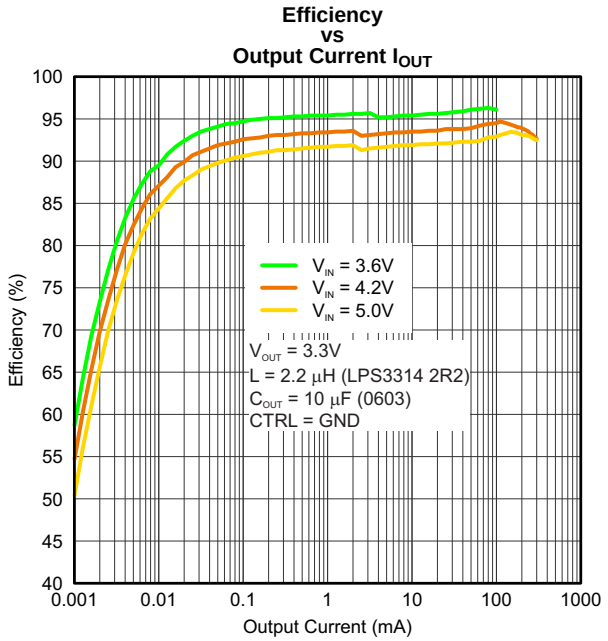


Figure 10. Efficiency V_{OUT} = 3.3V

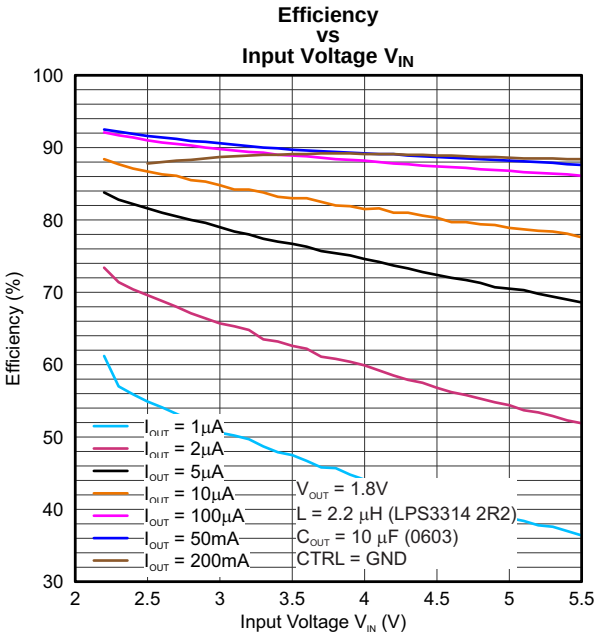


Figure 11. Efficiency V_{OUT} = 1.8V

TYPICAL CHARACTERISTICS (continued)

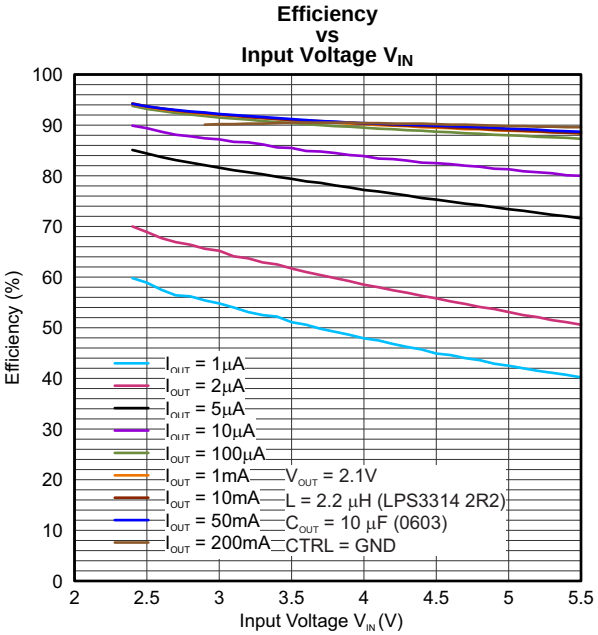


Figure 12. Efficiency V_{OUT} = 2.1V

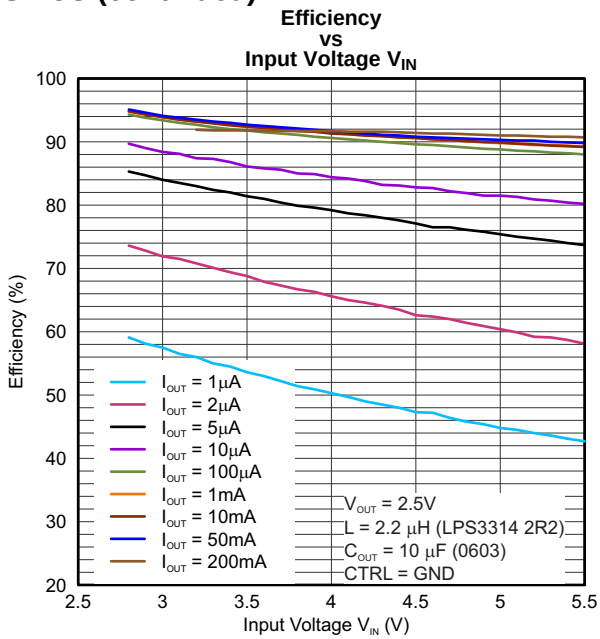


Figure 13. Efficiency V_{OUT} = 2.5V

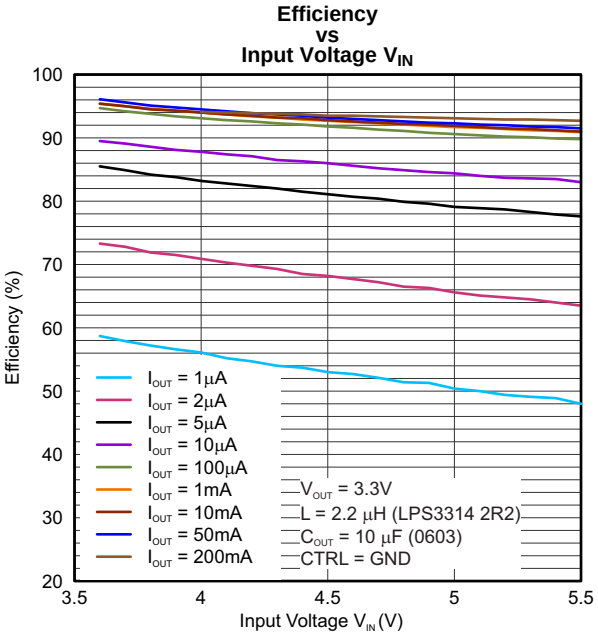


Figure 14. Efficiency V_{OUT} = 3.3V

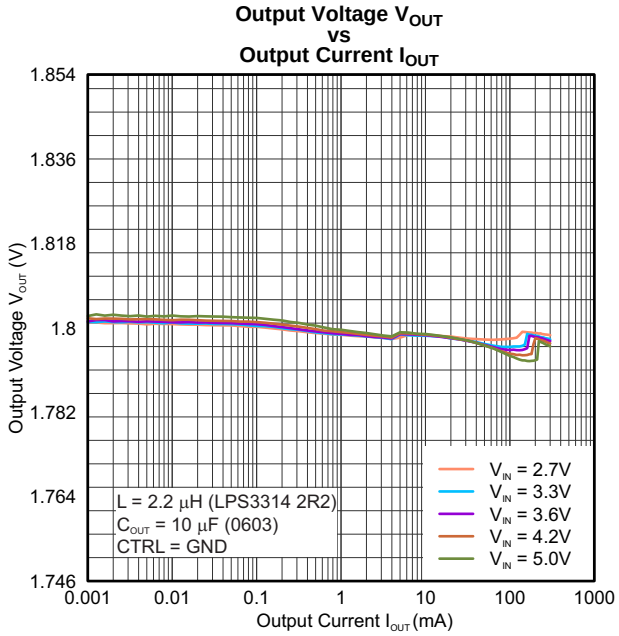


Figure 15. Output voltage V_{OUT} = 1.8V

TYPICAL CHARACTERISTICS (continued)

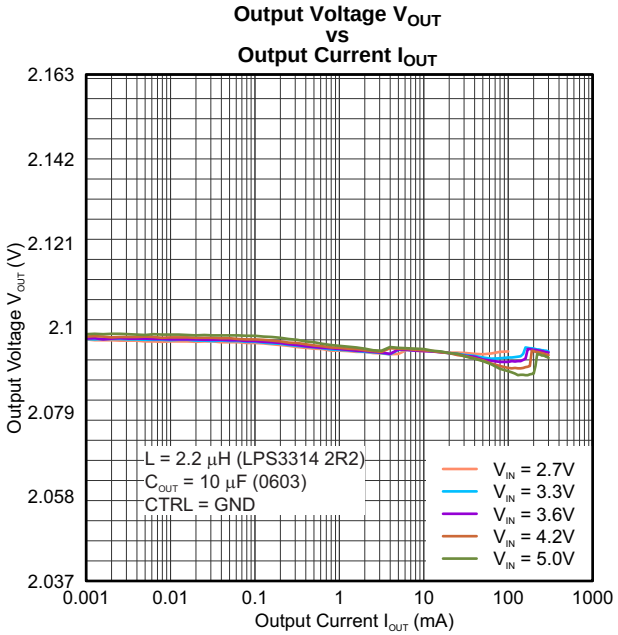


Figure 16. Output voltage V_{OUT} = 2.1V

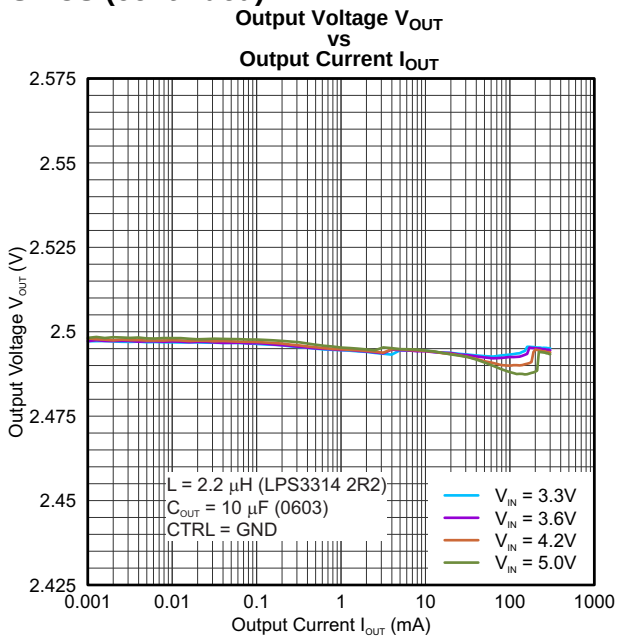


Figure 17. Output voltage V_{OUT} = 2.5V

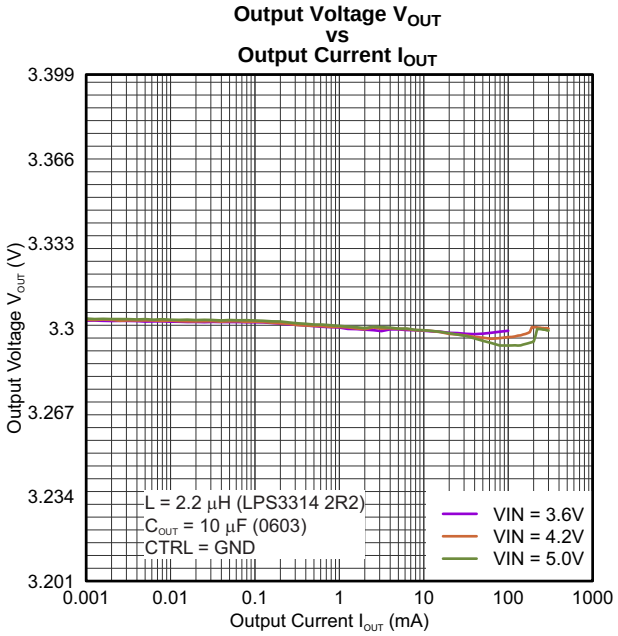


Figure 18. Output voltage V_{OUT} = 3.3V

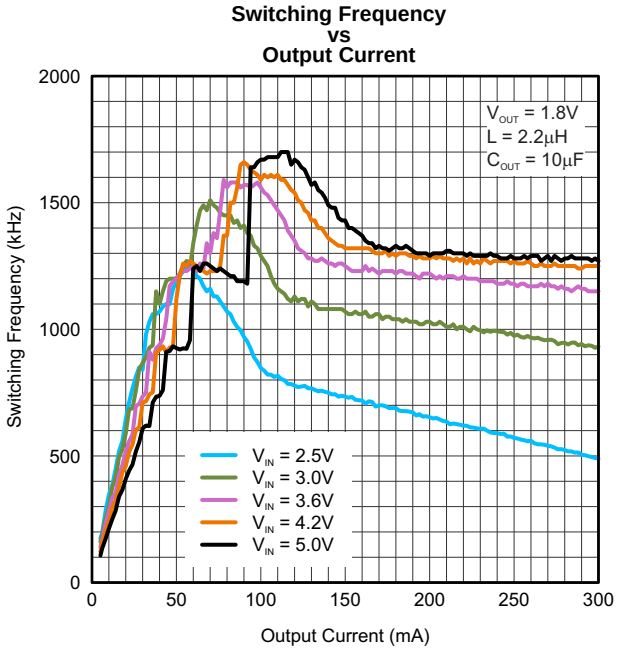


Figure 19. Typical switching frequency V_{OUT} = 1.8V

TYPICAL CHARACTERISTICS (continued)

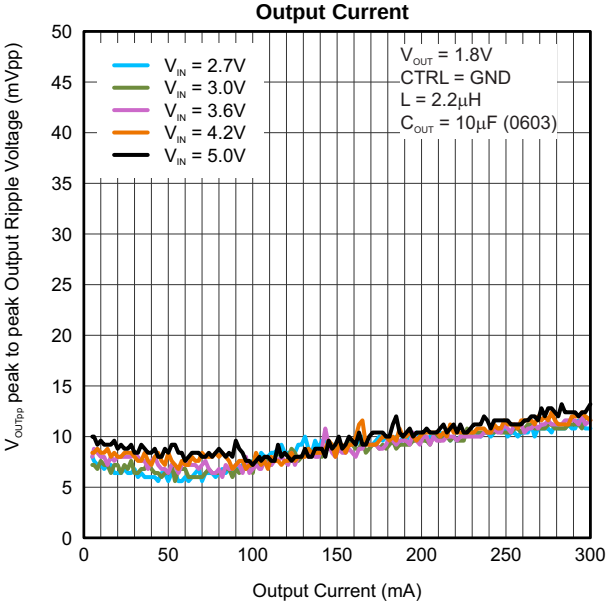


Figure 20. Typical output ripple voltage V_{OUT} = 1.8V

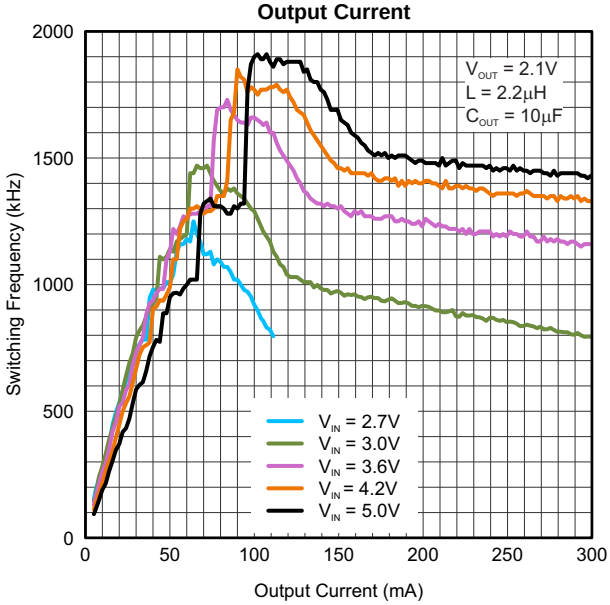


Figure 21. Typical switching frequency V_{OUT} = 2.1V

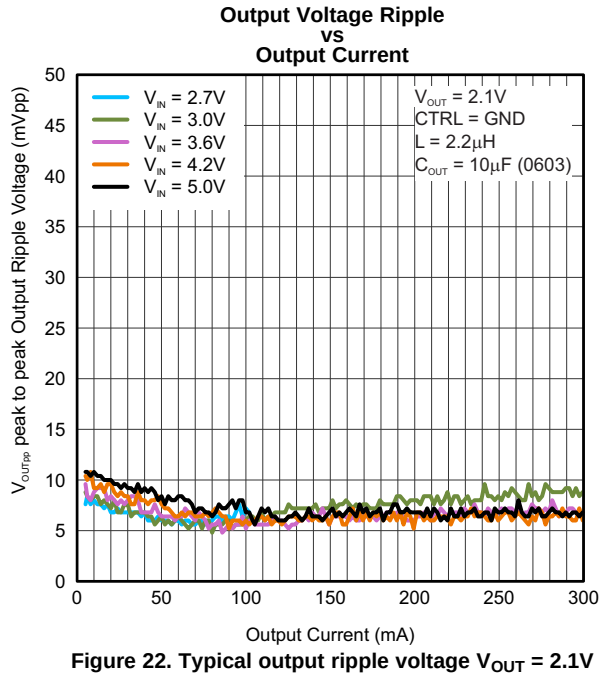


Figure 22. Typical output ripple voltage V_{OUT} = 2.1V

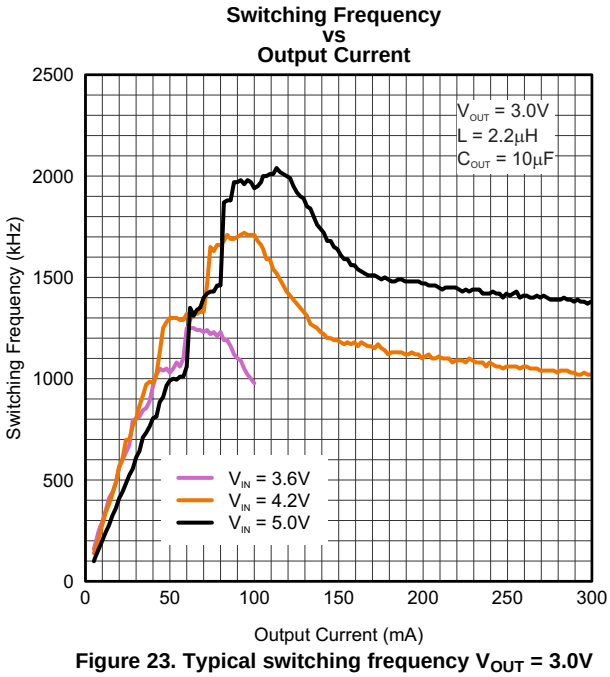


Figure 23. Typical switching frequency V_{OUT} = 3.0V

TYPICAL CHARACTERISTICS (continued)

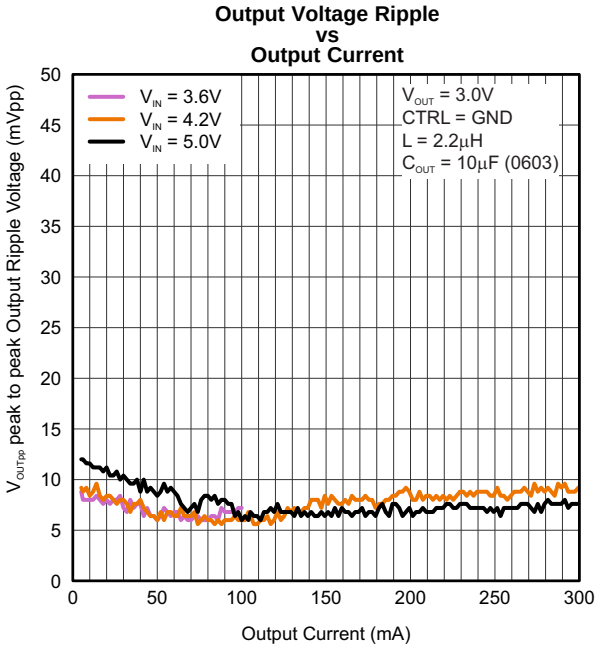


Figure 24. Typical output ripple voltage V_{OUT} = 3.0V

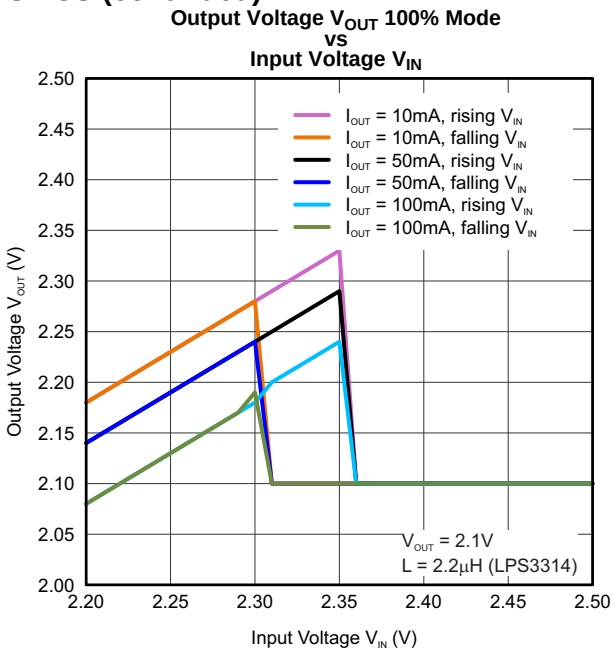


Figure 25. 100% mode transition V_{OUT} 2.1V

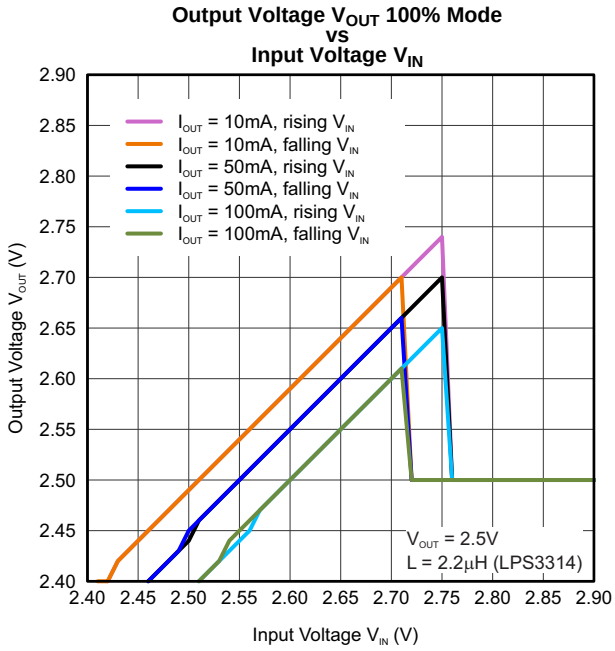


Figure 26. 100% mode transition V_{OUT} 2.5V

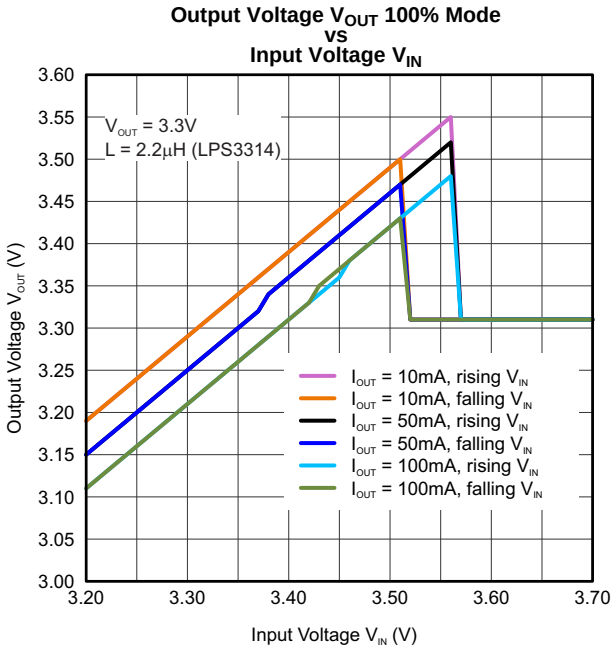


Figure 27. 100% Mode Transition V_{OUT} 3.3V

TYPICAL CHARACTERISTICS (continued)

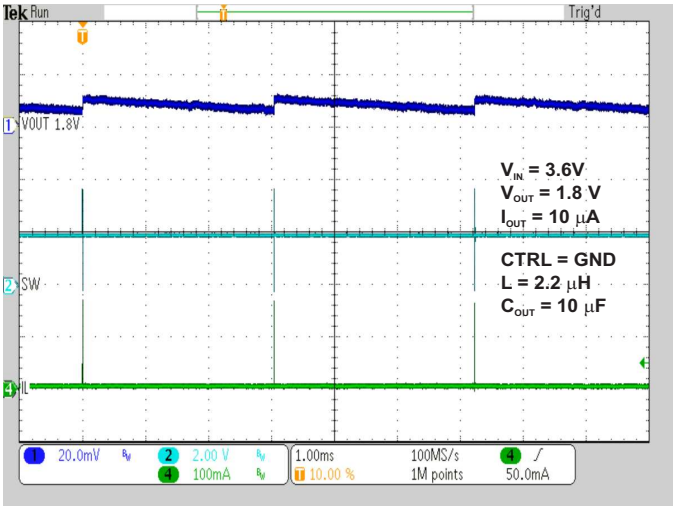


Figure 28. Typical operation I_{Load} = 10µA V_{OUT} = 1.8V

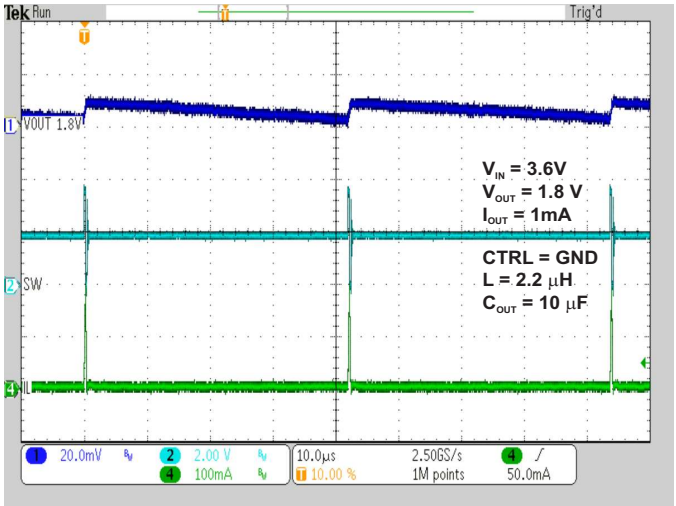


Figure 29. Typical operation I_{Load} = 1mA, V_{OUT} = 1.8V

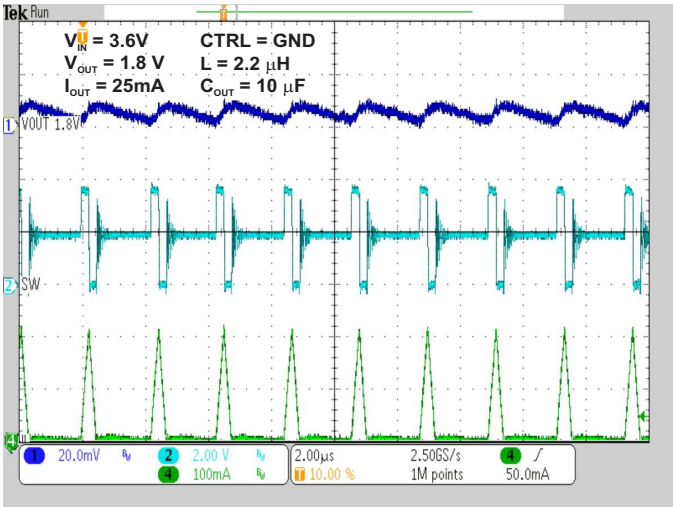


Figure 30. Typical operation I_{Load} = 25mA, V_{OUT} = 1.8V

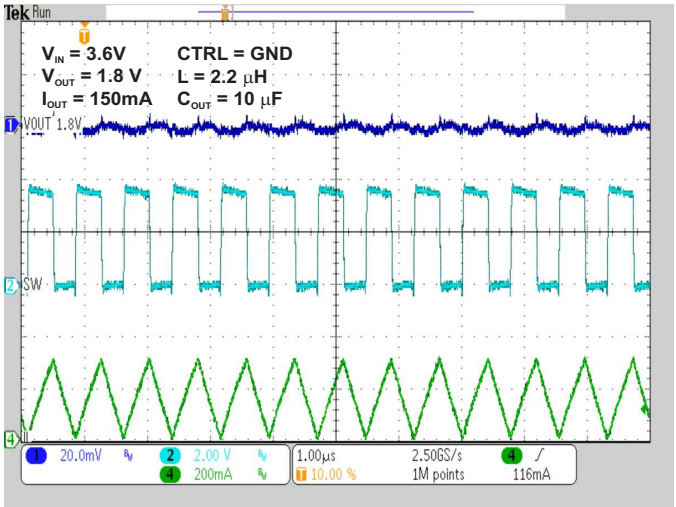


Figure 31. Typical operation I_{Load} = 150mA, V_{OUT} = 1.8V

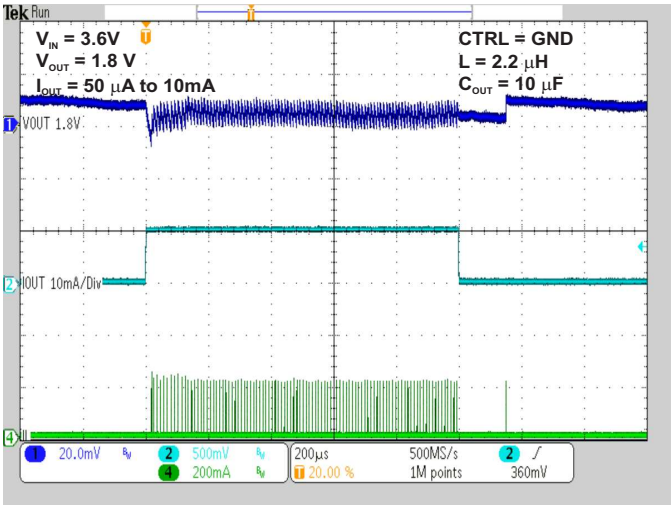


Figure 32. Load transient response V_{OUT} = 1.8V

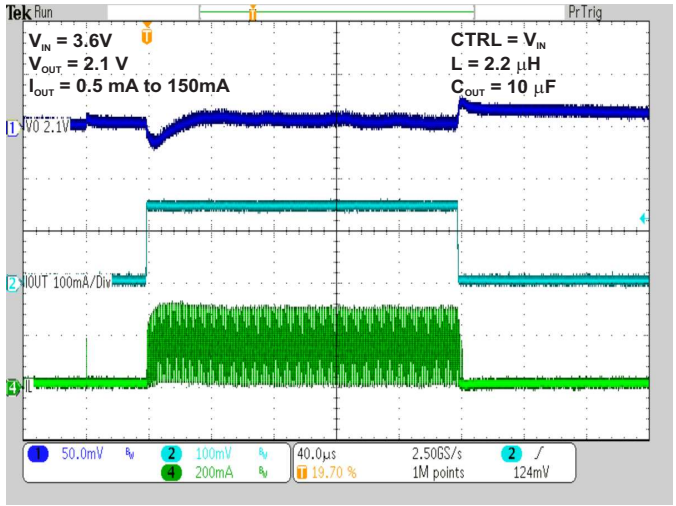


Figure 33. Load transient response V_{OUT} = 2.1V

TYPICAL CHARACTERISTICS (continued)

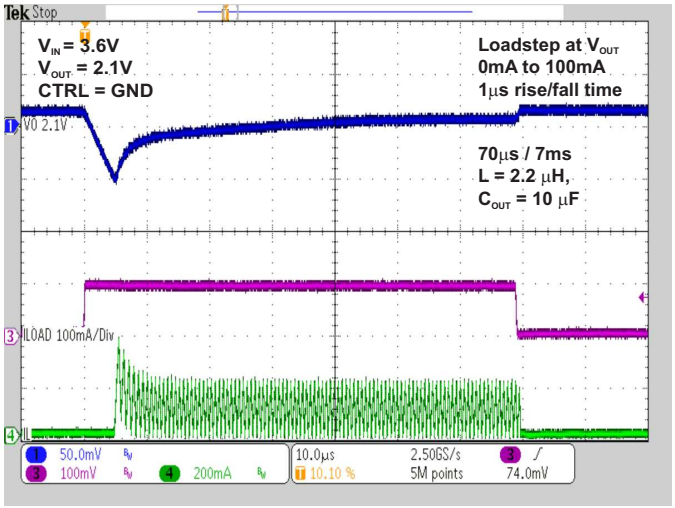


Figure 34. Load transient response CTRL = GND

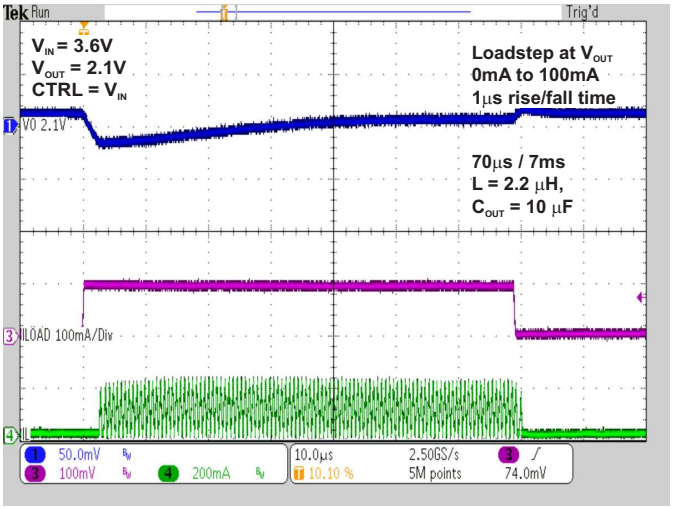


Figure 35. Load transient response CTRL = VIN

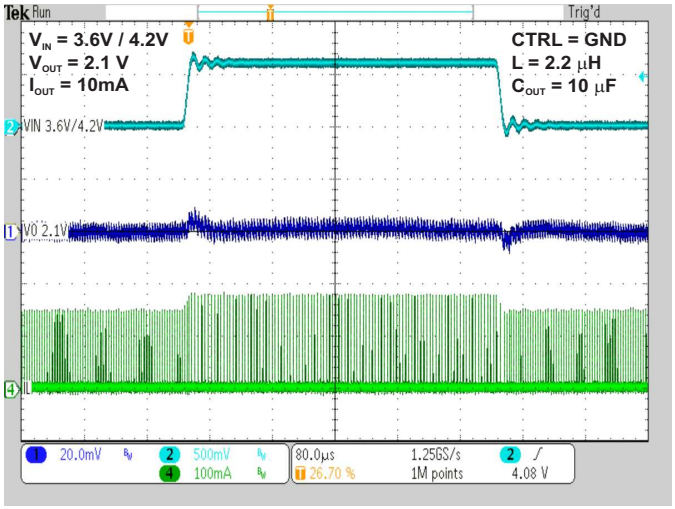


Figure 36. Line transient response I_{OUT}=10mA

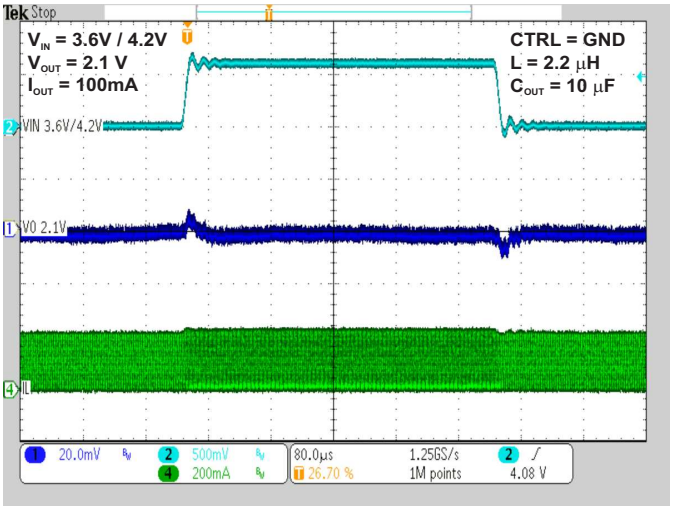


Figure 37. Line transient response I_{OUT}=100mA

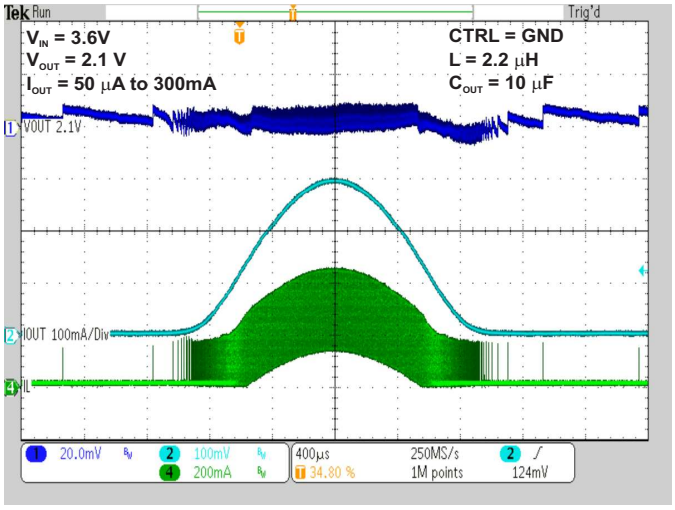


Figure 38. AC load sweep V_{OUT} = 2.1V

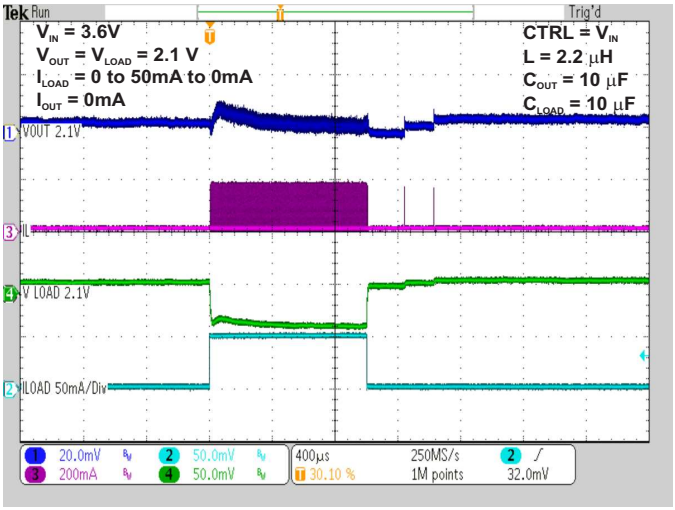


Figure 39. Load step at LOAD output

TYPICAL CHARACTERISTICS (continued)

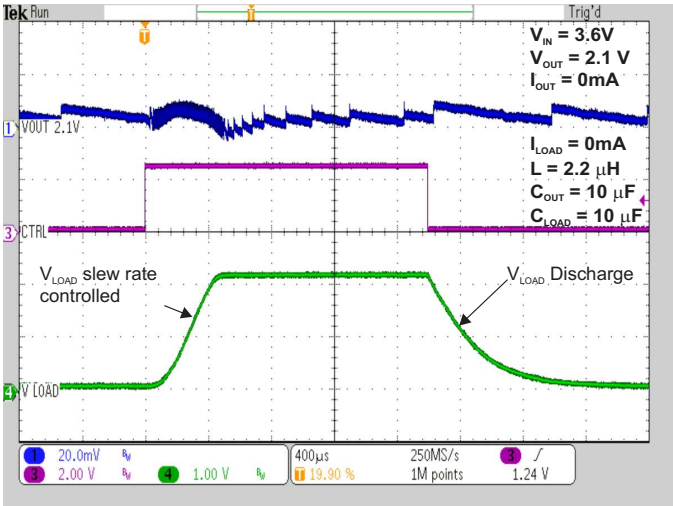


Figure 40. LOAD output ON / OFF

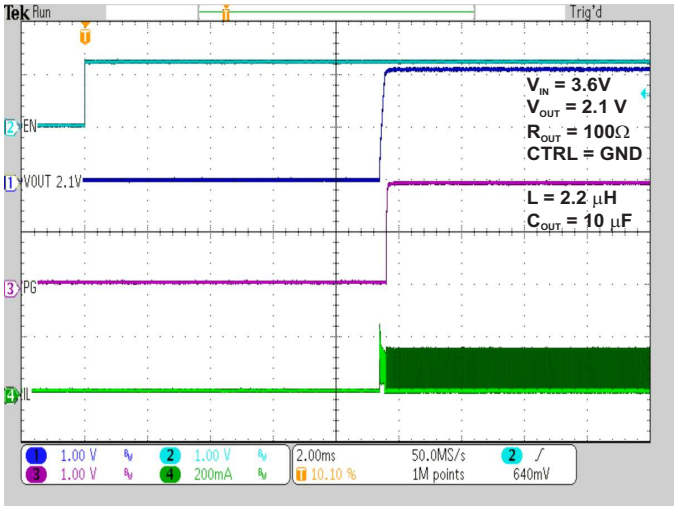


Figure 41. Device enable and start up

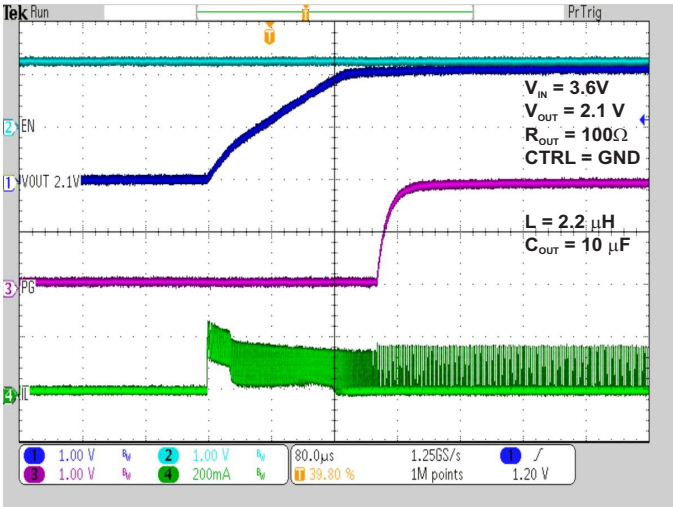


Figure 42. V_{OUT} ramp up after enable

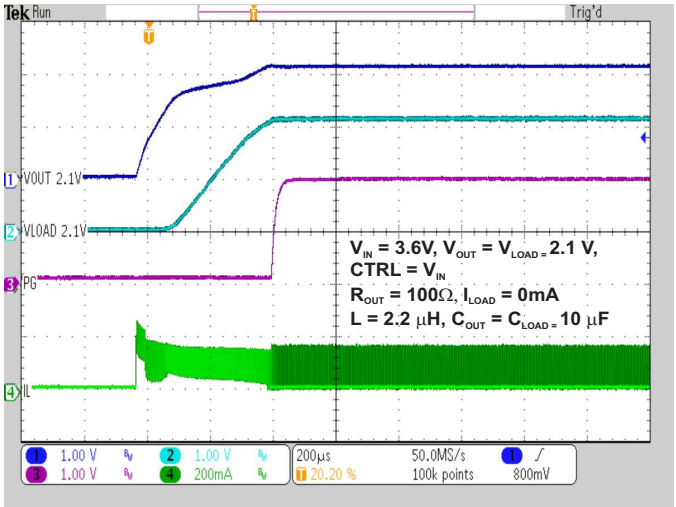


Figure 43. V_{OUT} ramp up with activated LOAD switch

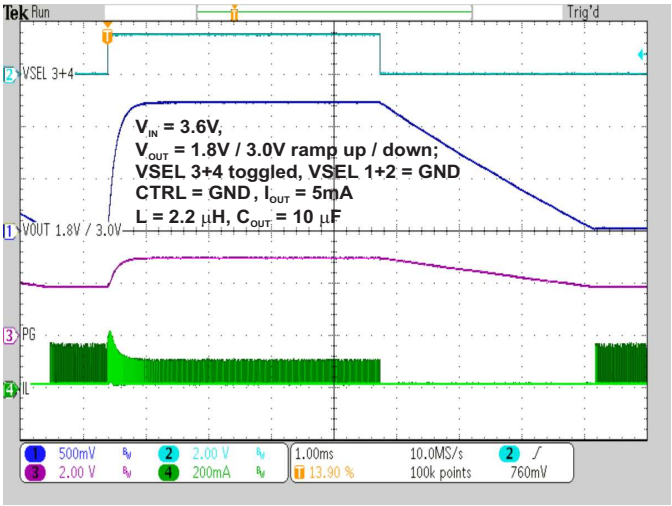


Figure 44. Dynamic output voltage scaling V_{OUT} = 1.8V/3.0V

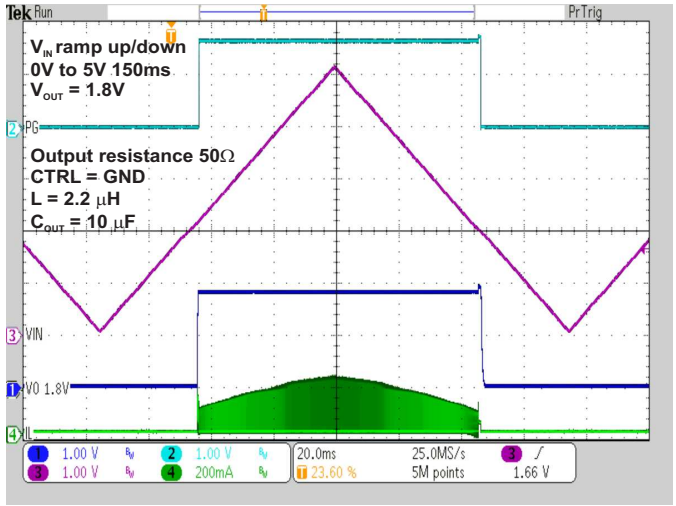


Figure 45. Input voltage ramp up/down V_{OUT} = 1.8V

TYPICAL CHARACTERISTICS (continued)

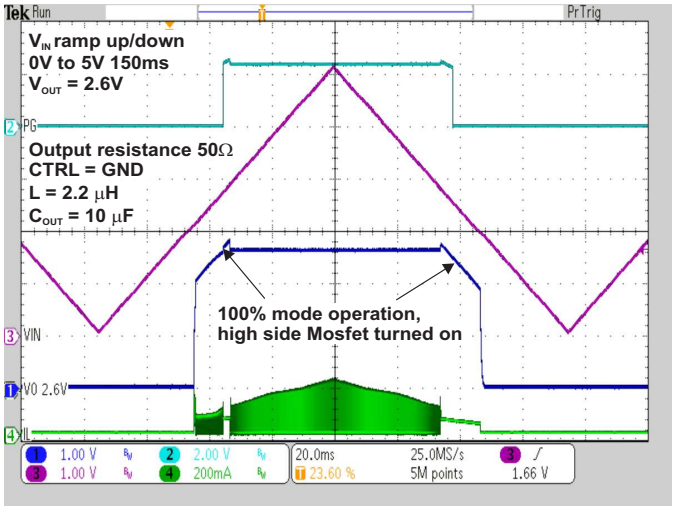


Figure 46. Input voltage ramp up/down V_{OUT} = 2.6V

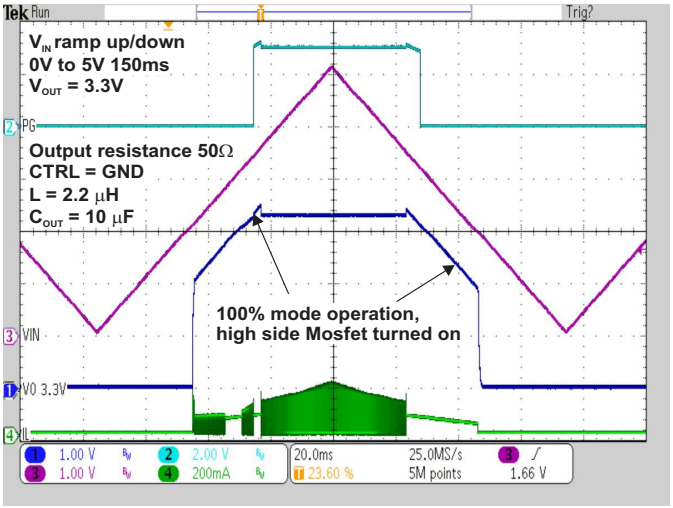


Figure 47. Input voltage ramp up/down V_{OUT} = 3.3V

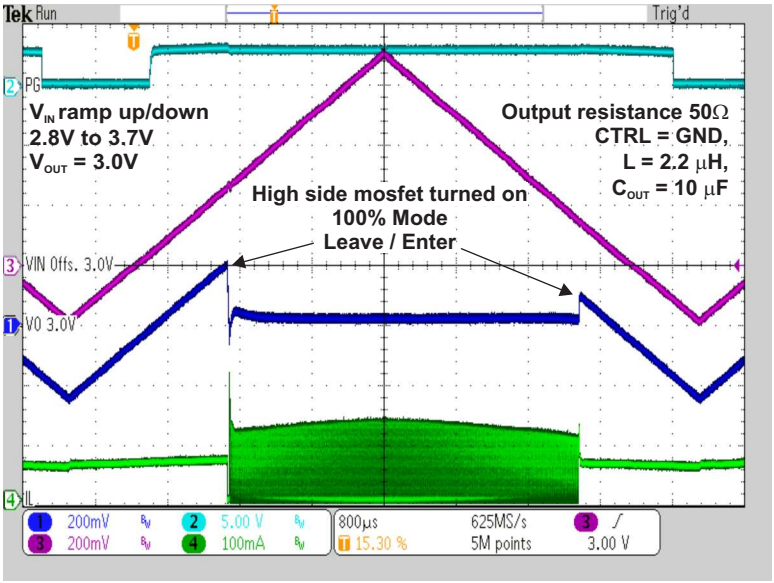


Figure 48. Enter/Leave 100% Mode operation

DETAILED DESCRIPTION

The TPS62740 is the first step down converter with an ultra low quiescent current consumption (360nA typ.) and featuring TI's DCS-Control™ topology while maintaining a regulated output voltage. The device extends high efficiency operation to output currents down to a few micro amperes.

DCS-Control™

TI's DCS-Control™ (Direct Control with Seamless Transition into Power Save Mode) is an advanced regulation topology, which combines the advantages of hysteretic and voltage mode control. Characteristics of DCS-Control™ are excellent AC load regulation and transient response, low output ripple voltage and a seamless transition between PFM and PWM mode operation. DCS-Control™ includes an AC loop which senses the output voltage (VOUT pin) and directly feeds the information to a fast comparator stage. This comparator sets the switching frequency, which is constant for steady state operating conditions, and provides immediate response to dynamic load changes. In order to achieve accurate DC load regulation, a voltage feedback loop is used. The internally compensated regulation network achieves fast and stable operation with small external components and low ESR capacitors.

The DCS-Control™ topology supports PWM (Pulse Width Modulation) mode for medium and high load conditions and a Power Save Mode at light loads. During PWM mode, it operates in continuous conduction. The switching frequency is up to 2MHz with a controlled frequency variation depending on the input voltage. If the load current decreases, the converter seamlessly enters Power Save Mode to maintain high efficiency down to very light loads. In Power Save Mode the switching frequency varies nearly linearly with the load current. Since DCS-Control™ supports both operation modes within one single building block, the transition from PWM to Power Save Mode is seamless without effects on the output voltage. The TPS62740 offers both excellent DC voltage and superior load transient regulation, combined with very low output voltage ripple, minimizing interference with RF circuits. At high load currents, the converter operates in quasi fixed frequency PWM mode operation and at light loads, in PFM (Pulse Frequency Modulation) mode to maintain highest efficiency over the full load current range. In PFM Mode, the device generates a single switching pulse to ramp up the inductor current and recharge the output capacitor, followed by a sleep period where most of the internal circuits are shutdown to achieve a lowest quiescent current. During this time, the load current is supported by the output capacitor. The duration of the sleep period depends on the load current and the inductor peak current.

During the sleep periods, the current consumption of TPS62740 is reduced to 360nA. This low quiescent current consumption is achieved by an ultra low power voltage reference, an integrated high impedance (typ. 50MΩ) feedback divider network and an optimized DCS-Control™ block.

CTRL / OUTPUT LOAD

With the CTRL pin set to high, the LOAD pin is connected to the VOUT pin via an load switch and can power up an additional, temporarily used sub-system. The load switch is slew rate controlled to support soft switching and not to impact the regulated output VOUT. If CTRL pin is pulled to GND, the LOAD pin is disconnected from the VOUT pin and internally connected to GND by an internal discharge switch. The CTRL pin can be controlled by a micro controller.

SOFTSTART

When the device is enabled, the internal reference is powered up and after the startup delay time $t_{Startup\_delay}$ has expired, the device enters softstart, starts switching and ramps up the output voltage. During softstart the device operates with a reduced current limit, $I_{LIM\_softstart}$, of typ. 1/4 of the nominal current limit. This reduced current limit is active during the softstart time $t_{Softstart}$. The current limit is increased to its nominal value, I_{LIMF}, once the softstart time has expired.

ENABLE / SHUTDOWN

The DC/DC converter is activated when the EN pin is set to high. For proper operation, the pin must be terminated and must not be left floating. With the EN pin set to low, the device enters shutdown mode with less than typ. 70nA current consumption.

POWER GOOD OUTPUT (PG)

The Power Good comparator features an open drain output. The PG comparator is active with EN pin set to high and V_{IN} is above the threshold V_{TH_UVLO+}. It is driven to high impedance once V_{OUT} trips the threshold V_{TH_PG+} for rising V_{OUT}. The output is pulled to low level once V_{OUT} falls below the PG hysteresis, V_{PG_hys}. The output is also pulled to low level in case the input voltage V_{IN} falls below the undervoltage lockout threshold V_{TH_UVLO-} or the device is disabled with EN = low. The power good output (PG) can be used as an indicator for the system to signal that the converter has started up and the output voltage is in regulation.

OUTPUT VOLTAGE SELECTION (VSEL1 - 4)

The TPS62740 doesn't require an external resistor divider network to program the output voltage. The device integrates a high impedance (typ. 50MΩ) feedback resistor divider network which is programmed by the pins VSEL 1-4. TPS62740 supports an output voltage range of 1.8V to 3.3V in 100mV steps. The output voltage can be changed during operation and supports a simple dynamic output voltage scaling, shown in Figure 44. The output voltage is programmed according to table Table 1.

VOUT AND LOAD DISCHARGE FUNCTION

Both the VOUT pin and the LOAD pin feature a discharge circuit to connect each rail to GND, once they are disabled. This feature prevents residual charge voltages on capacitors connected to these pins, which may impact proper power up of the main- and sub-system. With CTRL pin pulled to low, the discharge circuit at the LOAD pin becomes active. With the EN pin pulled to low, the discharge circuit at pin VOUT is activated.

AUTOMATIC TRANSITION INTO 100% MODE

Once the input voltage comes close to the output voltage, the DC/DC converter stops switching and enters 100% duty cycle operation. It connects the output VOUT via the inductor and the internal high side MOSFET switch to the input VIN, once the input voltage V_{IN} falls below the 100% mode enter threshold, V_{TH_100-}. The DC/DC regulator is turned off, not switching and therefore it generates no output ripple voltage. Because the output is connected to the input, the output voltage tracks the input voltage minus the voltage drop across the internal high side switch and the inductor caused by the output current. Once the input voltage increases and trips the 100% mode leave threshold, V_{TH_100+} , the DC/DC regulator turns on and starts switching again. See Figure 49.

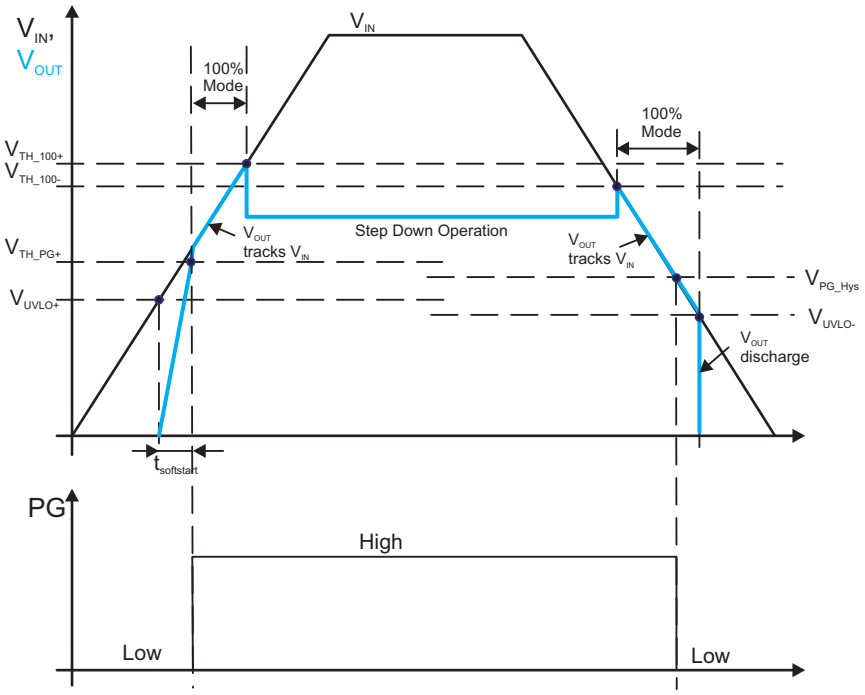


Figure 49. Automatic 100% mode transition

INTERNAL CURRENT LIMIT

The TPS62740 integrates a current limit on the high side, as well the low side MOSFETs to protect the device against overload or short circuit conditions. The peak current in the switches is monitored cycle by cycle. If the high side MOSFET current limit is reached, the high side MOSFET is turned off and the low side MOSFET is turned on until the current decreases below the low side MOSFET current limit.

APPLICATION INFORMATION

OUTPUT FILTER DESIGN (INDUCTOR AND OUTPUT CAPACITOR)

The TPS62740 is optimized for operation with a 2.2µH inductor and with 10µF output capacitor.

Table 2. Recommended LC Output Filter Combinations

Inductor Value [µH](1)	Output Capacitor Value [µF](2)		
	4.7µF	10µF	22µF
2.2	√	√(3)	√

(1) Inductor tolerance and current de-rating is anticipated. The effective inductance can vary by 20% and -30%.
(2) Capacitance tolerance and bias voltage de-rating is anticipated. The effective capacitance can vary by 20% and -50%.
(3) This LC combination is the standard value and recommended for most applications.

INDUCTOR SELECTION

The inductor value affects its peak-to-peak ripple current, the PWM-to-PFM transition point, the output voltage ripple and the efficiency. The selected inductor has to be rated for its DC resistance and saturation current. The inductor ripple current (ΔI_L) decreases with higher inductance and increases with higher V_{IN} or V_{OUT} and can be estimated according to Equation 1.

Equation 2 calculates the maximum inductor current under static load conditions. The saturation current of the inductor should be rated higher than the maximum inductor current, as calculated with Equation 2. This is recommended because during a heavy load transient the inductor current rises above the calculated value. A more conservative way is to select the inductor saturation current above the high-side MOSFET switch current limit, I_{LIMF}.

$$\Delta I_L = Vout \times \frac{1 - \frac{Vout}{Vin}}{L \times f} \quad (1)$$

$$I_{Lmax} = I_{outmax} + \frac{\Delta I_L}{2} \quad (2)$$

With:

f = Switching Frequency
L = Inductor Value
ΔI_L = Peak to Peak inductor ripple current
I_{Lmax} = Maximum Inductor current

In DC/DC converter applications, the efficiency is essentially affected by the inductor AC resistance (i.e. quality factor) and by the inductor DCR value. Increasing the inductor value produces lower RMS currents, but degrades transient response. For a given physical inductor size, increased inductance usually results in an inductor with lower saturation current.

The total losses of the coil consist of both the losses in the DC resistance (R_{DC}) and the following frequency-dependent components:

- The losses in the core material (magnetic hysteresis loss, especially at high switching frequencies)
- Additional losses in the conductor from the skin effect (current displacement at high frequencies)
- Magnetic field losses of the neighboring windings (proximity effect)
- Radiation losses

The following inductor series from different suppliers have been used:

Table 3. List of Inductors

INDUCTANCE [µH]	DCR [Ω]	DIMENSIONS [mm^3]	INDUCTOR TYPE	SUPPLIER
2.2	0.23	2.0 × 1.2 × 1.0	MIPSZ2012 2R2	FDK
2.2	0.115	2.0 x 1.2 x 1.0	MDT2012CH2R2	TOKO
2.2	0.12	2.5 x 2.0 x 1.2	MIPSA2520 2R2	FDK
2.2	0.145	3.3 x 3.3 x 1.4	LPS3314	Coilcraft

DC/DC OUTPUT CAPACITOR SELECTION

The DCS-Control™ scheme of the TPS62740 allows the use of tiny ceramic capacitors. Ceramic capacitors with low ESR values have the lowest output voltage ripple and are recommended. The output capacitor requires either an X7R or X5R dielectric. Y5V and Z5U dielectric capacitors, aside from their wide variation in capacitance over temperature, become resistive at high frequencies. At light load currents, the converter operates in Power Save Mode and the output voltage ripple is dependent on the output capacitor value and the PFM peak inductor current. A larger output capacitors can be used, but it should be considered that larger output capacitors lead to an increased leakage current in the capacitor and may reduce overall conversion efficiency. Furthermore, larger output capacitors impact the start up behavior of the DC/DC converter.

INPUT CAPACITOR SELECTION

Because the buck converter has a pulsating input current, a low ESR input capacitor is required for best input voltage filtering to ensure proper function of the device and to minimize input voltage spikes. For most applications a 10µF is sufficient. The input capacitor can be increased without any limit for better input voltage filtering.

Table 4 shows a list of tested input/output capacitors.

Table 4. List of Capacitors

CAPACITANCE [µF]	SIZE	CAPACITOR TYPE	SUPPLIER
10	0603	GRM188R60J106ME84	Murata

LAYOUT CONSIDERATIONS

As for all switching power supplies, the layout is an important step in the design. Care must be taken in board layout to get the specified performance. If the layout is not carefully done, the regulator could show poor line and/or load regulation, stability issues as well as EMI problems and interference with RF circuits. It is critical to provide a low inductance, impedance ground path. Therefore, use wide and short traces for the main current paths. The input capacitor should be placed as close as possible to the IC pins as well as the inductor and output capacitor. The VOUT line should be connected to the output capacitor and routed away from noisy components and traces (e.g. SW line). See Figure 50 for the recommended PCB layout.

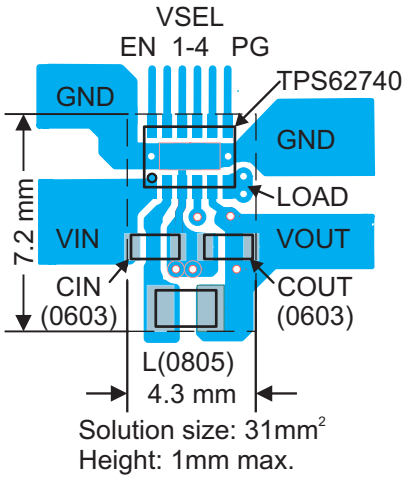


Figure 50. Recommended PCB Layout

TYPICAL APPLICATIONS

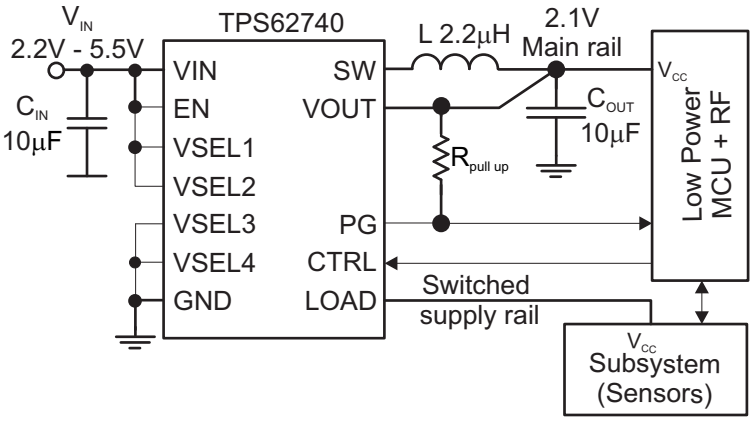


Figure 51. TPS62740 typical application circuit

EXAMPLES OF SYSTEM IMPLEMENTATIONS

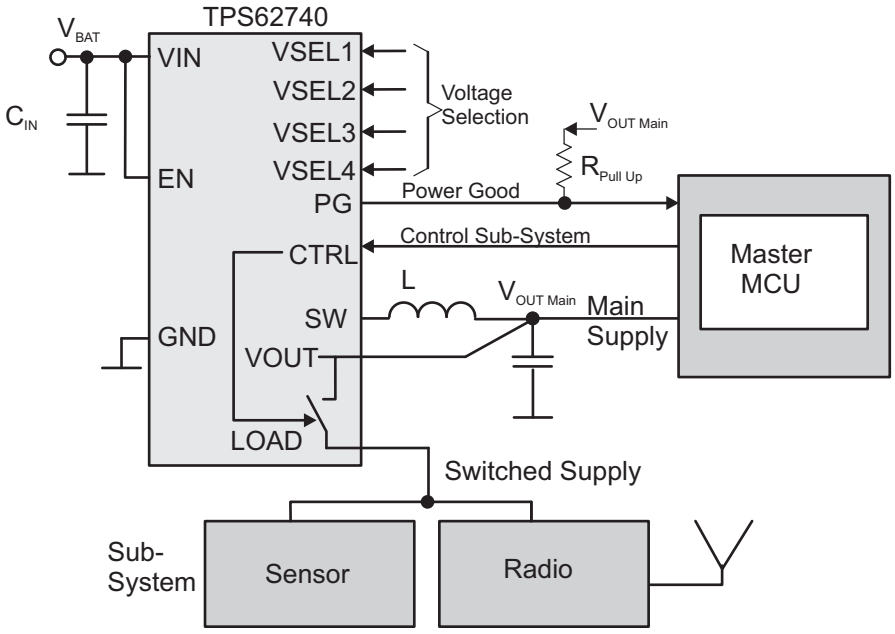


Figure 52. Example of implementation in a master MCU based system

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS62740DSSR	ACTIVE	WSON	DSS	12	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	62740	Samples
TPS62740DSST	ACTIVE	WSON	DSS	12	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	62740	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

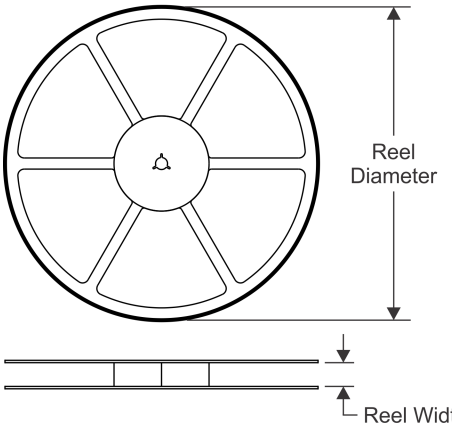
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

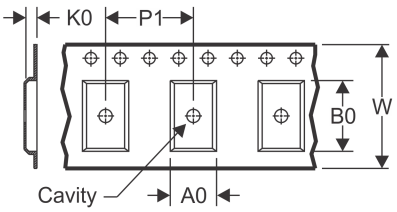
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

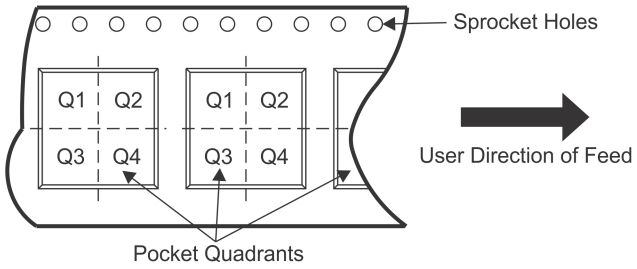


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

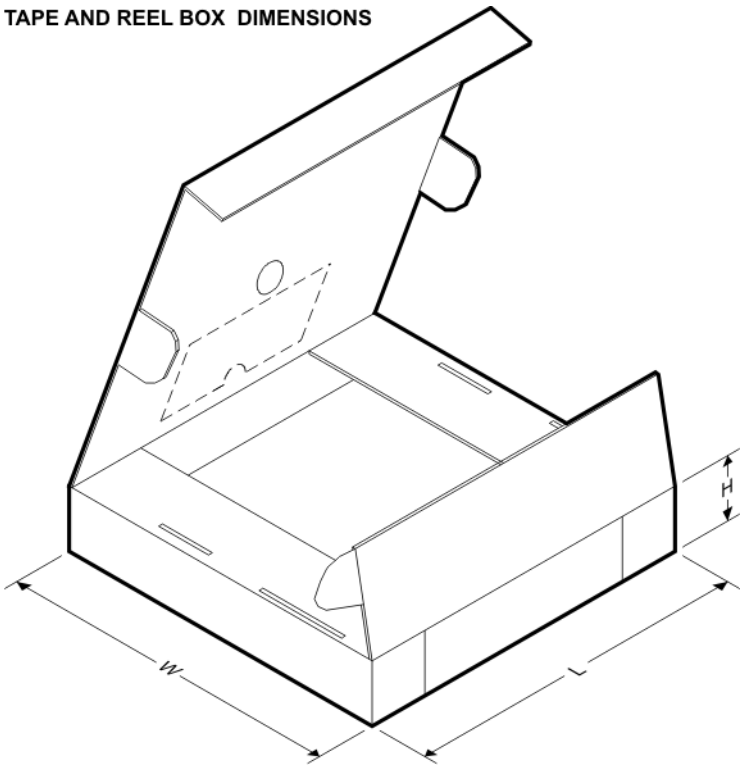
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS62740DSSR	WSON	DSS	12	3000	180.0	8.4	2.25	3.25	1.05	4.0	8.0	Q1
TPS62740DSST	WSON	DSS	12	250	180.0	8.4	2.25	3.25	1.05	4.0	8.0	Q1

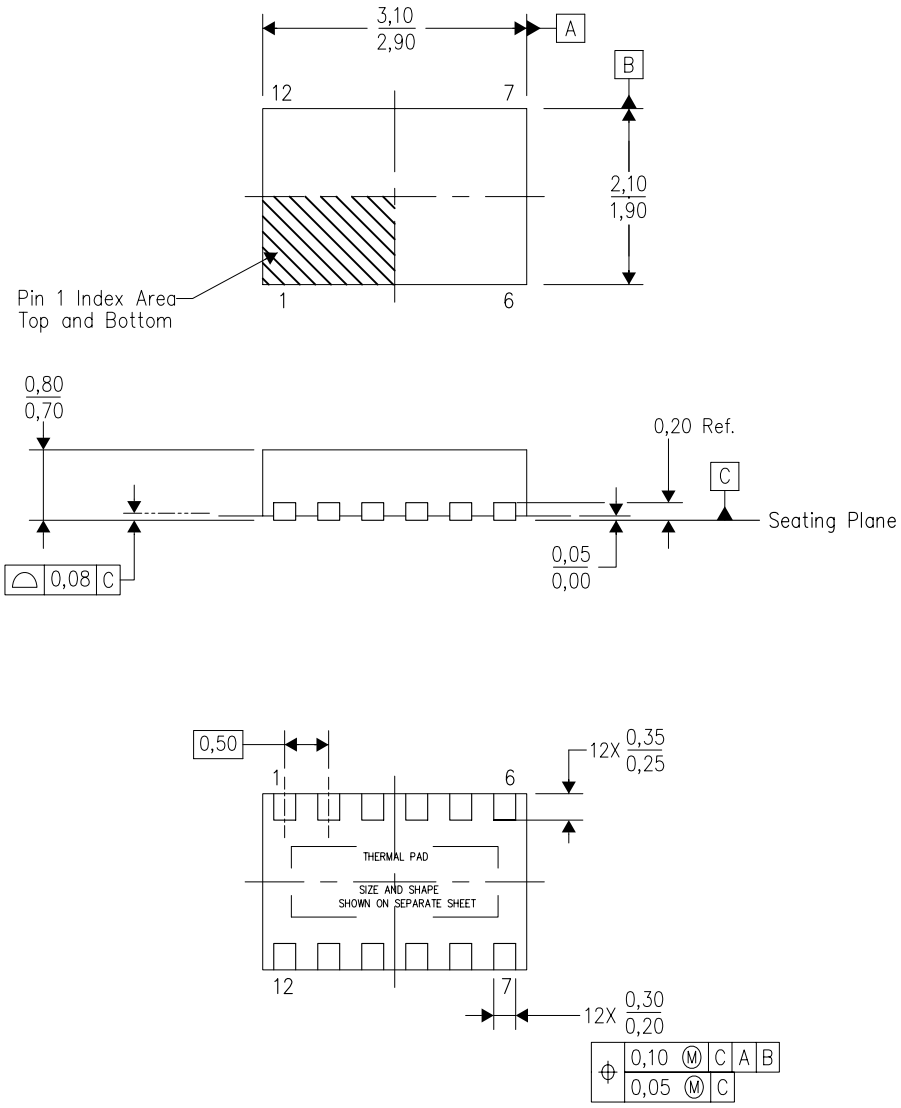
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS62740DSSR	WSON	DSS	12	3000	210.0	185.0	35.0
TPS62740DSST	WSON	DSS	12	250	210.0	185.0	35.0

DSS (R–PWSON–N12) PLASTIC SMALL OUTLINE NO–LEAD



4209244/C 07/11

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. SON (Small Outline No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

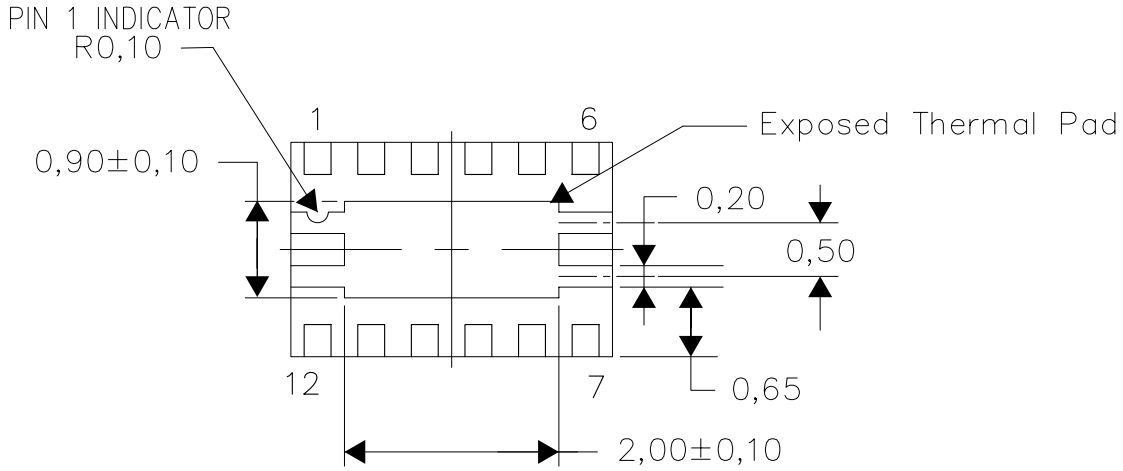
DSS (R–PWSON–N12) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



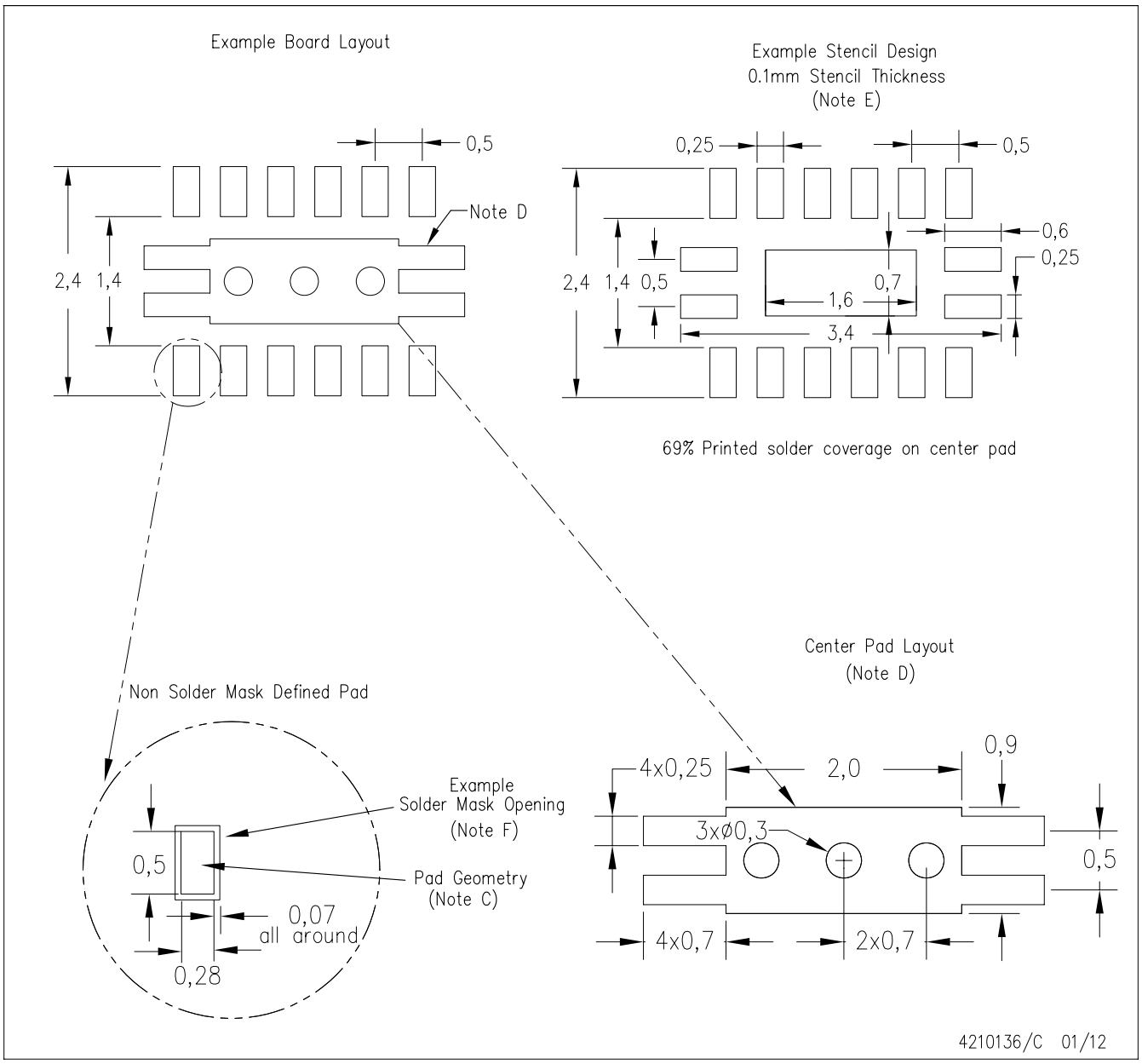
Bottom View

Exposed Thermal Pad Dimensions

4210135–2/C 02/12

NOTE: All linear dimensions are in millimeters

DSS (R–PWSON–N12) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265